



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Electrical Communications Engineering

Digital Phase Locked Loops

A Thesis submitted in partial fulfillment of the requirements of the
degree of
Master of Science in Electrical Engineering
(Electronics and Electrical Communications Engineering)

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

Digital Phase locked loops are important building blocks in modern system on chips containing digital, analog, and RF integrated circuits. As the frequency of operation of modern integrated circuits increases, the need for clean clock sources that consume low power and occupy small area becomes more critical. Digital phase locked loops provide a solution for low-jitter clocks without occupying much area compared to their analog counterparts.

This thesis presents the design of a wideband, low-jitter 5-GHz digital phase locked loop in a 65-nm CMOS process. The digital phase locked loop uses a high-resolution, low-power two-step time-to-digital converter to achieve a wide loop bandwidth with low jitter. The digital phase locked loop is designed with a loop bandwidth of 4-MHz using a 100-MHz reference. The digital phase locked loop employs a 13-bit hybrid $\Sigma\Delta$ digital-to-analog converter and a ring voltage-controlled oscillator to achieve a wide tuning range with a small frequency step.

Simulation results indicate that the digital phase-locked loop achieves a root-mean-square jitter and a peak-to-peak jitter of 1.59-ps and 20.69-ps, respectively at 5-GHz operation. The digital phase locked loop occupies an area of 0.026-mm² and consumes 4.5-mA from a 1.2-V supply.

Keywords - Digital phase-locked loop (DPLL), time-to-digital converter (TDC), delta-sigma digital-to-analog converter ($\Sigma\Delta$ -DAC), and digitally controlled oscillator (DCO).

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