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Low Power Serial Link Equalizer

A thesis
submitted in partial fulfillment of the requirements of the degree of Master of Science in Electrical Engineering

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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To My Family for their support and encouragement

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Thesis title: "**Low Power Serial Link Equalizer**"

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Thesis Summary

High speed serial data links can be used in many data wire-line communication standards as they solve synchronization problems resulting from using parallel data buses.

This thesis studies equalization techniques for low-power high-speed serial data at the receiver side at a data-rate of 8Gb/s. Two types of equalizers are proposed, linear equalizer (CTLE) followed by non-linear equalizer (DFE).

The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references and one appendix.

Chapter 1
It includes thesis introduction as well as definitions associated with high speed serial data links. This chapter states the reasons of using serial data links instead of the parallel ones, as well as the link components. This chapter ends with the thesis organization.

Chapter 2
This chapter contains a background for the channel parameters and the definition of BER. Introducing different types of equalization techniques of the high speed serial links in both transmitter and receiver sides. Previous work and state-of-the-art are also included.

Chapter 3
This chapter gives a brief description for the different equalization architectures in the receiver side including linear and non linear equalization with pros and cons. Previous work and state-of-the-art are also included.

Chapter 4
This chapter describes in details the system level of the proposed design, different architectures are demonstrated with their advantages and disadvantages. Complete analysis, design for each block are included.

Chapter 5
This chapter describes in details the block circuits' design for the proposed different architectures showing the simulation results of each block, the system level integration, and top-level simulations results.

Chapter 6

This chapter lists conclusions, summary and contributions of this work and offers some ideas for future work.

Supervisors:

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