



Ain Shams University

Faculty of Computers and Information Sciences

Computer Systems Department

Performance Analysis and Enhancement of Optical Interconnection Networks for High Performance Supercomputers

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By

Ahmad Muhammad Ahmad Mahany

B.Sc. in Computer and Information Sciences (2011),
Demonstrator at Computer Systems Department

Under Supervision of

Prof. Dr. Hossam Faheem

Professor
Computer Systems Department
Faculty of Computers and Information Sciences
Ain Shams University

Prof. Dr. Samy Ghoniemy

Professor
Faculty of Informatics and Computer Science
British University in Egypt

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This thesis is dedicated to my mother, i really can't describe you in a book. To the memory of my father. I really miss you, but I know that you are happy of this progress of my life. I always pray for you. Thanks to my brother, sister and my future wife. Without all of you, i could not complete that work.

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Abstract

Recent advances in the manufacturing of nano-photonic devices and optical networks on chip together with advanced optical routing can enable heterogeneous HPC systems of more than 1000 cores to efficiently perform terascale computing.

In this work, a Wavelength Division Multiplexed Photonic Network-on-Chip (WDM-PNoC) is proposed to replace the conventional electrical Network-on-Chip (NoC) of the homogeneous HPC systems and will be simulated on an IBM Blue Gene/q compute chip as a case study. The proposed WDM-PNoC is intended to reduce the performance limitations of homogeneous HPC systems and provide significant low latency, high bandwidth, and low power dissipation. A WDM-PNoC architecture for optical routing and switching is modeled and developed using a customized version of the PhoenixSim simulator. The proposed models are based on recent advancement in nano-photonics device fabrication, architecture design, CAD optimization and include on-chip optical light sources and modulators, photodetectors, buffers, switches, couplers, optical waveguides, and on-chip WDM devices.

Through a series of simulations, the efficiency of the proposed system is studied in terms of power and energy consumption, data transmission latency and throughput. Moreover, the design parameters of a commercial IBM Blue Gene/q compute chip were used to compare the overall system performance using its current conventional electrical architecture with WDM-PNoC architecture under synthetic random traffic with different loads. The proposed

architecture reduces the overall energy consumption by approximately 40% compared with the electronic one, and achieves an average decrease in end-to-end delay of approximately 60%, meanwhile it remarkably exceeds the offered throughput of the current commercial system.

An enhanced WDM-PNoC model is proposed by including an enhanced WDM-PNoC architecture, which reduces the overall energy consumption by approximately 40% when it is compared with the static WDM-PNoC without negatively affecting the end-to-end delay. The results also show the performance superiority of the proposed enhanced WDM-PNoC.

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