AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
ELECTRONICS AND COMMUNICATIONS DEPARTMENT

Memristor Modeling And its Applications in Digital Circuits

A thesis

Submitted in partial fulfillment of the requirements of the degree of Master of Science in **Electrical Engineering**

Submitted by

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B.Sc. of Electrical Engineering
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Cairo, 2014

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Thesis: Memristor Modeling And its Application in Digital Circuits

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Faculty of Engineering – Ain Shams University
Electronics and Communication Engineering Department

Thesis title: **"Memristor Modeling and its Applications in Digital Circuits"**

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ABSTRACT

This thesis aims to analyze and design different on-chip memristor based nonvolatile resistive random-access memory (RRAM) macros. Several memristor RRAM cells and architectures are proposed that allow for single bit and multiple-bit per cell storage. The thesis starts by proposing several proposed memristor models. These models were later tailored to be used in designing a complete 8x32 SRAM macro using a proposed RRAM cell consisting of two back-to-back memristors and one access MOSFET. This 1T2M cell has a high advantage over traditional 6T SRAM cells in terms of area and power dissipation, allowing for denser memories on the same area. As memristors are nonvolatile devices, their states remain unchanged even if the supply is disconnected. This gives a strong edge for memristor cells over conventional 6T CMOS SRAM cells that require a retention supply to maintain its stored data. Another RRAM architecture is proposed that allows the same 1T2M RRAM cell to be used for multi-bit storage, allowing for denser power efficient on-chip memories.

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Summary

The thesis is divided into six chapters as listed below:

Chapter 1
In this chapter, the motivation for this work is presented, as well as a high-level overview on memristors and SRAMs. This is later followed by the thesis outline.

Chapter 2
In this chapter, the operation of a memristor device is discussed in details

Chapter 3
This chapter focuses on modeling a memristor device. Several models such as the linear, non-linear and exponential models are presented, and compared using simulations.

Chapter 4
Chapter 4 gives an overview on 6T SRAM Module

Chapter 5
This chapter focuses on the design and analysis of a single bit memristor-based RRAM cell. The cell write operation, single read and repeated read modes are analyzed in details. This 1T2M memristor cell is then used to design a complete on-chip RRAM macro. Implementation details and simulation results are shown and compared to conventional 6T SRAM macros, as well as to other memristor based memory implementations previously proposed in the literature.

Chapter 6
In this chapter, we upgrade the cell used in the past chapter to be able to store multiple bits. A complete RRAM macro is designed to support multiple-bit storage per cell. Implementation details and simulation results are shown to compare it to the memristor-based RRAM proposed in the previous chapter.

Chapter 7
This chapter concludes the thesis and presents any planned future work.

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