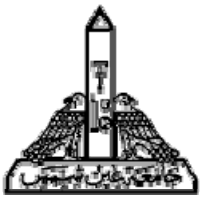

Ain Shams University
Faculty of Engineering

Electronics and Communication Engineering Department

A Compact Model for Nanoscale Transistors

A THESIS

Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

By

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STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

The work included in the thesis was carried out by the author at the Electronics and Communication Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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ABSTRACT

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Down-scaling of MOS devices is continuously attempted aiming to achieve faster circuit speed, smaller area, and lower power dissipation. Multi-gate MOSFET is one of the most promising semiconductor devices that was proven to be the best choice for future ICs, so, it has become an intense subject of scientific research.

This thesis addresses the different multi-gate structures and the recent compact models of the double gate structure. In this work, we study the physical effects of multi-gate MOSFETs. Moreover we review the different compact models of double-gate MOSFETs (Taur, Ortiz, Hu and Common Symmetric Multi-Gate models) stressing the advantages and disadvantages of each model. Finally, we introduce a new model based on Hu's model. Our new model introduces by a simple way modifying the energy states quantization effect without the need to solve Schrödinger's equation. In addition, we present how to include the velocity saturation, channel length and drain induced barrier lowering effects. These effects represent the most important short channel effects. Furthermore, we show an extraction flow to extract our proposed model parameters. We use the Nanomos device simulator results as a reference to apply our extraction flow. Finally, we validate the model continuity and compare its results with Hu's model.

Key Words: double gate MOSFETS, compact models, quantum confinement effect, short channel effects

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A^*	Suggested model parameter
α	Interaction factor representing the charge coupling between the two gates
α_1	Suggested model parameter
α_2	Suggested model parameter
beta	User specified quantity for Nanomos device simulator
β	Constant of x direction
β_d	β at the drain
β_s	β at the source
C_{ox}	Oxide capacitance per unit area
C_{ox}	The oxide capacitance
D_1	Suggested model parameter
D_2	Suggested model parameter
ΔV_{th}	Threshold voltage shift
$\Delta\phi_i$	The work function difference
E	Electric field
E_s	Surface electric field
E_{c0}	The original conduction band minimum of bulk silicon
$E_{//}$	The electric field in the transport direction
EI	Electrostatic Integrity (EI) factor
ε_{si}	Permittivity of silicon
ε_{ox}	Oxide permittivity
f	Dimensionless correction factor for Hu's model
$\hbar$	The reduced Planck constant
k	Boltzman's constant
L_{el}	Electrical channel length
L	The effective channel length
ℓ	The characteristic length
λt_{box}	Depth in the buried oxide
mu_low	User specified quantity for Nanomos device simulator
m^*	The electron effective mass
μ	Effective mobility
μ_o	Model parameter which presents the value low field mobility
n_0	Mobile electrons concentration at the center of silicon film
n	Mobile electrons concentration

n_i	Intrinsic carrier density
N_D^+	Ionized donors concentration
N_A^-	Ionized acceptors concentration
ψ	Electrostatic potential
ψ_0	Potential at the center of the silicon film
ψ_{SL}	The surface potential at the drain
ψ_{S0}	The surface potential at the source
ψ_{oL}	The potential at the center of the silicon film at the drain
ψ_{o0}	The potential at the center of the silicon film at the source
ψ_s	The surface potential
p	Mobile holes concentration
$\rho(x)$	Charge density
P_{I0}	The zero-order term of the parameter
P_{IL}	The length dependence parameter
P_{IT}	The silicon thickness dependence parameter
q_{in}	Normalized inversion charge
q_s	Normalized source inversion charge
q_d	Normalized drain inversion charge
q	Electron charge
Q_{in}	Inversion charge
r	Smoothing parameter
SC_1	Suggested model parameter
σ_1	Dimensionless factor which considers the drain induced barrier lowering
σ_2	Dimensionless factor which considers the short channel length
T	Temperature
t_{ox}	Oxide thickness
t_{dep}	Penetration depth of the gate field in the channel region
t_{si}	Silicon film thickness
vel_sat	User specified quantity for Nanomos device simulator
V_{ds}	Drain-to-source voltage
V_{bi}	Source or drain built-in potential
V	Electron quasi-Fermi potential
V_g	Gate voltage
V_s	Source voltage
V_d	Drain voltage
V_{gs}	Gate-to-source voltage

V_{fb}	Flat-band voltage
V_{GF}	The difference between the gate-to-source voltage and the flat-band voltage
v_{ch}	Normalized channel voltage
v_{g}	Normalized gate voltage
v_{d}	Normalized drain voltage
v_{bi}	Normalized built-in voltage
v_{sat}	A model parameter which presents the value of velocity saturation
v_{deff}	the effective drain voltage
w	Channel width
$W_0()$	The usual short-hand notation used for the principal branch of the ‘‘Lambert-W’’ function
x_{j}	Junction depth
X_{dep}	The depletion width in the substrate

Introduction

Multi-gate MOSFET is one of the most promising semiconductor devices that was proven to be the best choice for future ICs, so, it has become an intensive subject of scientific research.

This thesis aims to study the different multi-gate structures and the recent compact models of the double gate structure. In this work, a new compact model for the undoped symmetric double gate is introduced. This model includes the most important short channel effects and the quantum confinement effect. Furthermore, an extraction flow for the model parameters is suggested.

The thesis consists of three chapters, list of contents, figures as well as a list of references.

Chapter 1

In this chapter, an overview of the bulk MOSFET scaling challenges and the different multi-gate structures are presented. Moreover, the behavior of the multi-gate structures against the short channel effects is explained. In addition, the major advantages of the double-gate MOSFET over the bulk MOSFET are explained. Finally, the most important quantum mechanical effects encountered in double-gate MOSFETs are illustrated.

Chapter 2

In this chapter, the compact modeling concept is reviewed. Moreover, the most famous symmetric double-gate compact models (Taur, Ortiz, Hu and Common Symmetric Multi-Gate models) are presented stressing the advantages and disadvantages of each model. Finally, a brief overview on the device simulation and its advantages is given.

Chapter 3

In this chapter a new model based on Hu's model is proposed. Our new model is based on modifying the energy states quantization effect without the need to solve Schrödinger's equation. In addition, we present how to include the velocity saturation, channel length and drain induced barrier lowering effects. These effects represent the most important short channel effects. Furthermore, we show an extraction flow to extract our proposed model parameters. We use the Nanomos device simulator results as a reference to apply our extraction flow. Finally, we validate the model continuity and compare its results with Hu's model.

Finally, the thesis ends by extracting conclusions and stating future work that might be done based on this work.

CHAPTER 1

Literature Review

1.1 Introduction

Silicon-based microelectronic devices have revolutionized our world in the past five decades. The need for higher computing power at cheaper cost has fueled incessant the CMOS scaling. It all started with the invention of integrated circuits in late 1950's that revealed the possibility of using transistors in almost all kinds of electronic circuits. The next major breakthrough came with the demonstration of the first metal-oxide semiconductor field-effect transistor (MOSFET) in 1960 by Kahng and Atalla which would enable cost-effective integration of large number of transistors with interconnections on a single silicon chip. Five years later, Gordon Moore published his famous paper describing the evolution of transistor density in integrated circuits. He predicted that the number of transistors per chip would quadruple every three years [1]. This prediction became well known as Moore's law and has been remarkably followed by semiconductor industry for the last forty years. Fig. 1.1 shows the Moore's Law with regard to the number of transistors in Intel's microprocessors. A modern day microprocessor has about a billion transistors.

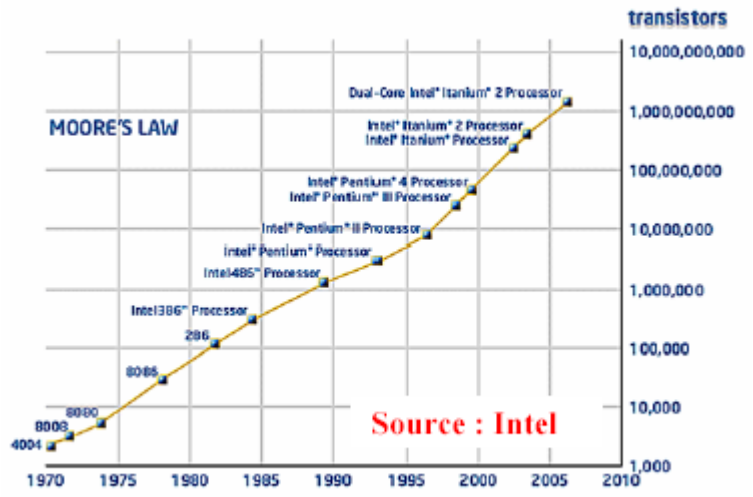

Figure 1. 1 Moore's Law in microprocessors.

Over the past three decades, by reducing transistor gate lengths with each new generation of manufacturing technology, steady improvements in circuit performance (speed) and cost per function have been achieved. However, continued transistor scaling will not be as straightforward in the future as it has been in the past because fundamental materials and process limits are rapidly being approached. For all practical purposes, it