Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department

DESIGN AND IMPLEMENTATION OF LDPC FOR DVB-S2

A Thesis
Submitted in partial fulfillment for the requirements of the degree of Master of Science in Electrical Engineering

(Electronics and Communications Engineering)

Submitted By

Hend Ahmed Orabi
B. Sc. Electronics & Communications Engineering

Supervised By

Prof. Dr. Abdelhalim Zekry
Electronics and Communications Engineering Department,
Faculty of Engineering, Ain Shams University

Dr. Gehan Gomaa
Electronics and Communications Engineering Department,
Faculty of Engineering, Ain Shams University

Cairo 2014

Judgment Committee

Name: Hend Ahmed Orabi Mohamed

Thesis: Design and implementation of LDPC for DVB-S2

Degree: Master of Science in Electrical Engineering

Title, Name and Affiliation **Signature**

Prof. Dr. Talaat Abdel Latief El Garf ……

(Professor in Higher Technological Institute
in tenth of ramadan)

Prof. Dr. Wagdy Refaat Anis ……

(Professor in Ain-shams University, Faculty of Engineering
,Electronics and Communications Department)

Prof. Dr. Abdelhalim Abdelnaby Zekry ……

(Professor in Ain-shams University, Faculty of
Engineering ,Electronics and Communications Department)

Date: / /

First and last, there are no words that can express my deep thanks to Allah. Thank you very much.

`

ACKNOWLEDGMENT

My sincere and deep thanks to my beloved father, mother, and my husband Eng. Hany Raafat for their continuous support, guidance and encouragement.

My deepest gratitude and appreciation to my thesis advisors Prof. Dr. Abdelhalim Zekry for his continuous guidance, encouragement and support throughout my work and in the paper writing. I am truly indebted and thankful for his great efforts that helped me to bring this thesis to fruition.

Especial gratitude to my friends Eng. Moshera, Eng. Amera, Eng. Allam Shihata, Eng. Amin Al-Said, Eng. Ahmed Abd Elrahman and Eng. Mohamed Hawary for their technical support and encouragement. Many thanks to all friends and colleagues in Thebes Academy.

Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department

STATEMENT

This dissertation is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in thesis was carried out by the author at the laboratories of the department of Engineering and Scientific Instrument, Nuclear Research Center, Atomic Energy Authority.

No part of this thesis has been submitted for a degree or qualification at any other university or institute.

Name : Hend Ahmed Orabi

Signature :

Date :

Ain Shams University

Faculty of Engineering

Electronics and Communications Engineering Department

Curriculum Vitae

Name of Researcher	:	Hend Ahmed Orabi Mohamed
Date of Birth	:	14-3-1988
Place of Birth	:	Egypt
Nationality	:	Egyptian
First University Degree	:	B.Sc in Electronics and Communication Engineering, Thebes Higher Institute for Engineering
Certification Date	:	May 2009

ABSTRACT

The Low-Density Parity-Check (LDPC) codes are gaining high attention in Channel Coding field these days. LDPC codes are the best forward error correcting codes which achieve very good performance close to the Shannon limit. This advantage makes these codes to be used for real implementation for some applications such as DVB-S2 which is a satellite broadcasting standard that needs high performing codes as it is sensitive to time.

In this thesis, we focus our research on the iterative decoding algorithms for LDPC codes. First, we study the algorithm of hard-decision decoding and its modified versions which reduce the bit error rate with less complexity. Second, we study the performance of the soft-decision decoding algorithm. The Sum-Product Algorithm (SPA) is an example of soft decision algorithm that gives superior performance among all other algorithms but with more complexity than hard-decision algorithms.

However, one of the main problems facing usage of these codes in communication systems is the high complexity decoding algorithms that results in high decoding delay. Such delay is not acceptable in some applications that depend on time such as video transmission. So, the third type of algorithms, studied in this thesis, is the hybrid-decision decoding algorithm. This algorithm provides a trade off performance and complexity between those of the soft and hard decision algorithms when they are compared with each other. Two-stage Hybrid decision decoding algorithm introduces better performance than hard decision and less complexity and delay than SPA.

This thesis presents MATLAB simulation results where the performance of the three decoding algorithms (hard, soft, hybrid) is measured by the bit error rate versus the signal-to-noise ratio for additive white Gaussian noise channel (AWGN). Also in this thesis, hardware implementation technique for the three algorithms using VHDL language is presented. The resource utilization and delay time is compared between them.

SUMMARY

This thesis presents the design and implementation of LDPC for DVB-S2 using MATLAB and VHDL respectively. The rest of the thesis is organized as follow:

Chapter one: This chapter contains an introduction to the digital video broadcasting (DVB) systems with a brief review on the error correcting codes and their types. Finally, this chapter introduces an overview about VHDL language that can be used to implement LDPC.

Chapter two: This chapter shows the design of LDPC encoder with MATLAB simulation. Also, the chapter contains the design of LDPC decoders with comparison between all decoding algorithms using MATLAB simulation (compared to the uncoded system that contains modulation block only). Finally, the discussion of using LDPC codes for DVB-S2 (second generation of Digital video broadcasting for satellite) is presented.

Chapter three: This chapter presents the implementation of modulation and demodulation blocks using VHDL language. Also, the chapter contains the implementation of LDPC encoder and some types of decoder using Xilinx program where the comparison between three decoding types is presented at the end of the chapter.

Finally, Conclusion and future work are presented in Chapter 4 where the main points summarizing the thesis are shown. References are presented at the end of the thesis.

Table of Contents

List of Figures

List of Tables