Ain Shams University
Faculty of Engineering
Electronics and Communications Department

Design of high performance ADC

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

Submitted by:

Ahmed Salah Hashim Ibrahim
B.Sc. of Electrical Engineering
(Electrical and Communications Department)
Ain Shams University, 2005.

Supervised by:

Prof. Dr. Hisham Sayed Ramadan Haddara
Ain Shams University

Prof. Dr. Kahled Wageh Sharaf
Ain Shams University

Cairo 2012

Statements

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

The work included in the thesis was carried out by the author at the Electronics and Communication Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

Name: Ahmed Salah Hashim Ibrahim
Signature:
Date:

Curriculum Vitae

Name of Researcher	Ahmed Salah Hashim Ibrahim
Date of Birth	24-May-1983
Place of Birth	Egypt
First University Degree	B.Sc. in Electrical Engineering
Name of University	Ain Shams University
Date of Degree	June 2005

Acknowledgments

All praise is due to Allah.

I want to thank my supervision committee, Prof. Dr. Hisham Sayed Ramadan Haddara and Prof. Dr. Kahled Wageh Sharaf for their support and guidance during my work in this thesis.

Also I would like to thank Eng. Yousry Elmaghraby for his help in formatting this thesis in LaTeXand for introducing the layout tools of Cadence for me. Eng. Mohamed Mohsen for the valuable discussions about the pipeline ADCs which helped me during this work.

Also I would like thank all my colleagues in Silicon Vision for their continuos help and support to complete this work efficiently.

And finally I would like to thank my parents for encouraging and supporting me in my life. And my wife for her endless patience and support till I finished this work.

Abstract

Ahmed Salah Hashim, Design of high performance ADC
Faculty of Engineering, Ain Shams University
2012

This thesis contains a description for the techniques used in the design of the pipeline ADC with the focus on the low voltage low power architectures.

The presented pipeline ADC operates from 1.2-V at 50-MSample/s and has a programmable resolution from 7 to 10 bits which help in reducing the power in the systems that supports multi-standard when high resolution is not required from the ADC. The ADC including the sample and hold amplifier (SHA) is using only 3 opamps to provide the max resolution, where each opamp is shared between 2 stages, this reduces both the total area and power of the ADC.

The ADC is implemented on 0.13μm CMOS technology and achieves 0.3 LSB differential non linearity (DNL), 0.3 LSB integral non linearity, 54.26 dB signal to noise and distortion ratio (SNDR) and consumes 10.5mW in the 10 bits mode of operation.

Contents

Table of contents **V**

List of figures **IX**

List of tables **XIII**

List of symbols and abbreviations **XV**

1 Introduction **1**
1.1 Motivation 3
1.2 Thesis organization 4

2 ADC Basics **5**
2.1 Ideal ADC 5
2.1.1 ADC transfer function 7
2.2 Quantization errors 7
2.3 Sampling clock jitter 9
2.4 ADC DC specifications 12
2.4.1 Differential non linearity (DNL) 12
2.4.2 Integral non linearity (INL) 12
2.4.3 Offset error 13
2.4.4 Gain error 13

2.4.5 Monotonicity 14
2.5 ADC frequency domain specifications 15
2.5.1 Signal to noise ratio (SNR) 15
2.5.2 Spurious free dynamic range (SFDR) 16
2.5.3 Total harmonic distortion (THD) 16
2.5.4 Signal to noise and distortion ratio (SNDR) 17
2.5.5 Effective number of bits (ENOB) 17
2.5.6 Effective resolution bandwidth (ERB) 18

3 ADCs architectures **19**
3.1 Flash ADC 19
3.1.1 Sources of errors in the flash ADC 21
3.1.2 Averaging 21
3.1.3 Interpolation 22
3.2 Two step flash 23
3.2.1 Sources of errors in the two step flash ADC 25
3.3 Folding ADC 25
3.3.1 Sources of errors in the Folding ADC 26
3.4 Pipeline ADC 28
3.4.1 Sources of errors in the pipeline ADC 28
3.5 Oversampled sigma Delta ADC 29
3.6 Successive approximation ADC 30
3.7 Time interleaved ADC 31
3.7.1 Sources of errors in the time interleaved ADC . . . 32

4 Pipeline ADC system **33**
4.1 Operation of pipeline ADC 33
4.2 Digital error correction 37
4.3 Pipeline ADC stage implementation 42
4.4 Sources of errors in the pipeline ADC 44
4.4.1 Gain errors 45
4.4.2 Settling error 51

4.5 Low power techniques in pipeline ADC 53
4.5.1 Opamp sharing 53
4.5.2 Stage scaling 55
4.6 Low voltage techniques in switches 55
4.6.1 Bootstrapped switches 56
4.7 Optimum stage resolution 57
4.7.1 Area 58
4.7.2 Power 59
4.7.3 Accuracy 60

5 Pipeline ADC circuit design **61**
5.1 Choosing the ADC input range 61
5.2 Choosing the ADC stages resolution 61
5.3 ADC top level 63
5.4 Circuit implementation 67
5.4.1 Sample and Hold circuit 68
5.4.2 1.5 bits pipeline stage 71
5.4.3 2.5 bits pipeline stage 75
5.4.4 3 bits flash ADC 78
5.4.5 Digital error correction 78
5.4.6 Clock generator 81
5.4.7 Reference buffer 81
5.5 Layout 83
5.6 Simulation results 90
5.6.1 ADC linearity simulation results 90
5.6.2 ADC circuit noise simulation results 93
5.6.3 ADC INL & DNL simulations results 95

6 Conclusion and suggested future work **99**
6.1 Conclusion 99
6.2 Suggested future work 101

A Simulink model and MATLAB code **103**
A.1 ADC simulink model 103
A.2 INL & DNL computation code 105

References **107**

List of Figures

1.1 Generic System block diagram 1
1.2 Multi standard receiver 2

2.1 Ideal ADC Block diagram 5
2.2 Ideal ADC transfer function 6
2.3 Quantization error 7
2.4 Quantization error PDF 8
2.5 Amplitude error due to sampling clock jitter 10
2.6 Non ideal ADC transfer function with DNL & INL errors . 13
2.7 ADC offset & gain errors 14
2.8 20MSPS ADC output spectrum 15

3.1 Flash ADC block diagram 20
3.2 Averaging scheme 22
3.3 Flash ADC with interpolation 23
3.4 Two step flash ADC 24
3.5 Folding ADC: (a)Folding ADC, (b)Folding circuit output . 26
3.6 Pipeline ADC architecture 27
3.7 Oversampled sigma delta ADC 29
3.8 Successive approximation ADC 30
3.9 Time interleaved ADC 31

4.1 Pipeline ADC (a)Block diagram, (b)Pipeline stage In/Out c/cs 35
4.2 Pipeline ADC output calculation 37
4.3 Pipeline ADC stage output (a)Without sub ADC offset, (b)With sub ADC offset 38
4.4 Pipeline ADC stage output with reduced stage gain (a)Without sub ADC offset, (b)With sub ADC offset 39
4.5 Pipeline first stage output and the corresponding digital output of 2 stage pipeline ADC 39
4.6 Pipeline ADC stage output after shifting the sub ADC decision levels 40
4.7 Pipeline ADC stage output after removing the last comparator of the sub ADC 41
4.8 ADC output calculation for the pipeline ADC with digital error correction 42
4.9 1.5 bit stage MDAC 42
4.10 Multi bit stage MDAC 44
4.11 The effect of gain error on the stage output 45
4.12 Effect of stage resolution on the matching accuracy 50
4.13 f_{unity}/fs for different stage resolution 53
4.14 Pipeline stage with opamp sharing 54
4.15 Ron of the transmission gate 56
4.16 Bootstrapped switch 57
4.17 Ratio of total area with the stage resolution for 10 bits ADC 60

5.1 ADC top level in the 10 bits mode 64
5.2 ADC top level in the 9 bits mode 64
5.3 ADC top level in the 8 bits mode 65
5.4 ADC top level in the 7 bits mode 65
5.5 Sample and Hold circuit 67
5.6 Bootstrapped switch 68
5.7 Opamp core 69

5.8 CMFB circuit 70
5.9 1.5 pipeline stage 72
5.10 Modified bootstrapped switch 73
5.11 3 levels flash ADC used in 1.5 pipeline stage 74
5.12 Dynamic comparator 75
5.13 2.5 pipeline stage 76
5.14 7 levels flash ADC used in 2.5 pipeline stage 77
5.15 3 bits flash ADC used in the last stage 79
5.16 DEC used in the pipeline ADC 80
5.17 Clock generator 81
5.18 References buffers 82
5.19 Layout floor plan 82
5.20 ADC Layout 83
5.21 Stage 1 layout 84
5.22 Stage 2 layout 85
5.23 Stage 3 layout 86
5.24 Reference voltage buffer layout 87
5.25 Common mode buffer layout 88
5.26 3 bits flash ADC layout 88
5.27 Clock generator layout 89
5.28 Digital error correction layout 89
5.29 ADC output spectrum in the 10 bits mode 91
5.30 ADC output spectrum in the 9 bits mode 91
5.31 ADC output spectrum in the 8 bits mode 92
5.32 ADC output spectrum in the 7 bits mode 92
5.33 Stage linear model used in noise analysis 93
5.34 ADC linear model used in noise analysis for the 10 bits mode 94
5.35 INL simulation results 96
5.36 DNL simulation results 97

A.1 1.5b pipeline stage simulink model 104
A.2 DEC simulink model 104

List of Tables

1.1 ADC requirements for different applications 2
1.2 Survey for ADC dynamic range requirements for different wireless standards 3

4.1 List of symbols 34
4.2 Capacitor mismatch simulation results in 0.13μm technology 51

5.1 ADC blocks configuration in different modes of operation 66
5.2 ADC SQNDR simulation results summary 93
5.3 ADC SNR simulation results summary 95
5.4 ADC SNDR & ENOB simulation results summary 95
5.5 Performance summary 97
5.6 Performance comparison with recently reported pipeline ADCs 98

6.1 Performance summary 100