AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Digital Equalization for High Speed Serial Links

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

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(Electronics Engineering and Electrical Communications)

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.
The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

Chapter One : This chapter gives the motivation, objectives and outline of the thesis.

Chapter Two: In this chapter, theoretical background about high speed serial links and their importance is presented. The issues that face high speed data transmission over serial links and different techniques used to mitigate these issues are discussed.

Chapter Three : In this chapter, the system-level design of the digital equalizer is presented.

Chapter Four: In this chapter, the RTL implementation of the multi-standard Gbps all-digital serial link equalizer is presented.

Chapter Five: This chapter contains the simulation and synthesis results for the design as well as FPGA prototyping results.

Chapter Six: This chapter contains the thesis conclusion and the possible future work.

Key words: Equalizer, ISI, Channel, Loss, FFE, DFE, high speed, serial links, Gigabit per second, multi-standard

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List of Abbreviations

ADC	Analog-to-Digital Converter
BER	Bit Error Rate
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibels
DCD	Duty Cycle Distortion
DFE	Decision Feedback Equalizer
DSP	Digital Signal Processing
DUT	Device Under Test
EMI	Electromagnetic Interference
FFE	Feed Forward Equalizer
FIFO	First In First Out
FIR	Finite Impluse Response
FPGA	Field Programmable Gate Array
FRE	Full Rate Equalizer
Gbps	Giga Bits Per Second
HPF	High Pass Filter
IIR	Infinite Impluse Response
ISI	Intersymbol Interference
LE	Linear Equalizers
LMS	Least Mean Square
MSE	Mean Square Error
PDF	Probability Density Function
VCO	Voltage Controlled Oscillator
RLS	Recursive Lease Squares
RTL	Register Transfer Level
SLE	Single Lane Equalizer
MHz	Mega Hertz
MUX	Multiplexer
mW	Milli Watt
UI	Unit Interval

Chapter One
Introduction

This chapter gives the motivation, objectives and outline of the thesis.

1.1 Motivation

With the continuous advances in silicon technologies and rapid increase of processor speeds and computing capabilities, there is a continuous need to achieve higher transmission data rates over backplane channels [1]. The required data rates now are in the order of Giga bits per second. These high data rates are required to be transmitted serially over a single channel in order to reduce the pin count and area of the transceiver chip. At the same time, low-cost channel materials are used in the manufacturing of channels. These low-cost channels have a narrow bandwidth compared to that of the high data rate transmitted digital signal. This narrow bandwidth is a result of the conductor skin depth and dielectric losses at frequencies above 1 GHz.

Other channel impairments include reflections due to impedance discontinuities and crosstalk between different channels. As a result, the transmitted signal suffers from high attenuation of its high frequency components when passing through the channel. This causes the transmitted symbol width to widen to more than one unit interval (UI). Hence, each symbol will interfere with its neighboring symbols, an effect called Inter-symbol Interference (ISI). This effect causes bit errors to take place in the received data bits causing the transmission to become unreliable.

In order to combat the ISI effect of limited-bandwidth channels to achieve high data throughput with low bit error rate (BER), data must be processed using a generic technique called equalization. This technique has different types and flavors. It can be done at transmitter before sending the data, or at the receiver after sending the data or both. It can also be done in analog domain or digital domain.

Transmitter-based equalization is often referred to as pre-emphasis. It is mainly a sort of high pass filtering done before transmitting the data to give an amplitude boost for the high frequency component in order to overcome the channel attenuation. It has the disadvantage of attenuating low frequency content due to peak power limitation. Moreover, it cannot be adaptable to different channels and varying operating conditions.

Receiver-based equalization can be sub-categorized into linear equalization and decision feedback equalization. Linear equalization is again high-pass filtering the received signal, while decision

feedback equalization tries to subtract the distortion caused on the symbol due to ISI. Receiver-based equalization has many advantages and few disadvantages compared to transmitter based one. They will be discussed in details in the next chapter.
Receiver-based equalization can be done in the analog domain on the received distorted symbols. The other option is to convert this analog signal into a digital signal using a high speed analog-to-digital converter (ADC). The equalization can then be done in the digital domain using digital signal processing techniques.
Digital signal processing has many advantages over analog signal processing. This includes easier programmability, greater flexibility, more powerful signal processing which translates into higher performance in terms of lower BER. Moreover, digital circuits are more robust to process, voltage and temperature variations than analog circuits. Most importantly, they can be easily ported into newer technology nodes which allows for easy area and power scaling. Analog circuits on the other hand need to be redesigned for technology migrations, some analog circuit components dimensions do not scale with technology node. As a result, there is a shift towards digital equalization where an ADC can be easily designed. This work is focused on the design of a digital equalizer that can work up to data rate of 10 Gbps for high-loss channels.

1.2 Thesis Objectives

This thesis focuses on the digital design implementation of low power high speed serial link receiver equalizer. This objective can be detailed as follows

1. System level design of high speed serial link ADC based receiver and testing against channel models with different attenuation profiles.
2. Design and implementation of all digital low power high speed serial link receiver equalizer that supports multiple bit rates up to 10 Gbps. The thesis presents both adaptive and blind equalization solutions.
3. FPGA prototyping of a slow version of the equalizer.

1.3 Thesis Outline

The thesis is organized as follows.
In chapter two, theoretical background about high speed serial links, channel characterization parameters, channel impairments and equalization is presented.