Ain Shams University – Faculty of Engineering
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C-based high-level synthesis using SystemC

A Thesis

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Computer Engineering.

The work included in this thesis was carried out by the author at the Computer and Systems Engineering Department, Faculty of Engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or qualification at other university or institution.

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ABSTRACT

C-BASED HIGH LEVEL
SYNTHESIS USING SYSTEMC

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Master of Science in Computer Engineering

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Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology promises new levels of system integration onto a single chip but also presents significant challenges to the chip designers who see current design tools and methodologies as inadequate for developing million gates ASICs from scratch. There is considerable pressure to keep design team size and design schedules constant even as design complexities grow.
Design ruse is the use of pre-designed and pre-verified cores and taken to be the most promising opportunity to bridge the gap between the available gate count and designer productivity.

In this thesis, we focus on using SystemC, a new modeling methodology based on C++, to describe an effective methodology for creating reusable designs to be used in a system-on-chip (SOC) and shows how through adapting linting rules and guidelines, the developer will be able to create reusable designs efficient in terms of quality and with higher performance.

For this thesis, we design a complete synthesis flow; start by parsing the input SystemC, estimate the logic and area consumed by desing, map the RTL logic to Xilinx technology and write the corresponding EDIF gate netlist to be taken as an input for Xilinx Place and Route tool. Also the system gets benefit from the existing VHDL-based tool through transferring the input synthesizable SystemC models into corresponding synthesizable VHDL models.

Keywords: SoC, SystemC, Design reuse, ASIC.

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GLOSSARY[1]

ASIC. Application Specific Integrated Circuit. An IC created for a dedicated purpose.

Design reuse. The ability to reuse portions of existing circuitry in new designs. When design cores are sold to a customer for reuse, it is sometimes referred to as intellectual property (IP).

HDL: Hardware Design Language. A method of writing a textual description of a circuit's behavior that becomes the specification for that circuit or module. HDL can be simulated and subsequently synthesized into gates. The most common HDLs are Verilog and VHDL.

Hierarchical design. The creation of a higher level of abstraction, often represented by a black box that can be defined later (top down design) or first (bottom up design).

IP (Intellectual Property). A reference to the marketing of pre-designed electronic cores for use in a customer's own designs. Cores can either be soft, such as HDL descriptions not yet synthesized, or hard already deployed in silicon or as gate level descriptions. Soft cores have the advantage that they are tool and foundry independent.

Logic simulator. A software application that simulates the operation of digital circuitry in order to perfect its operation before it's actually produced or prototyped.

RTL. Register Transfer Level. A style of HDL that describes circuit behavior in a structured fashion that more closely resembles logic elements. Most synthesis tools require HDL to be in RTL format before they can process it.

System on Chip (SoC). Advances in silicon processing technology enable integration of ever more complex systems on a single chip. These so-called Systems on Chip contain dedicated hardware components, programmable processors, memories, requiring not only the design of digital hardware but also the design of embedded software.

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[1] This Glossary focuses mainly on EDA terminology presented in chapter 1.