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Design and Implementation of RF CMOS Power Amplifiers for Bluetooth

By

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To The Soul of My Father

And

To My Mother

STATEMENT

This dissertation "Design and Implementation of RF CMOS Power Amplifiers for Bluetooth" is submitted to Ain Shams University for the degree of Doctorate of Philosophy in Electronics Engineering.

The work included in this thesis was carried out by the author in the Department of Electronics and Communications Engineering, Faculty of Engineering, Ain Shams University, from Oct. 1998 to Oct. 2004.

No part of this thesis has been submitted for a degree or a qualification at any other University or Institution.

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Abstract

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"Design and Implementation of RF CMOS Power Amplifiers for Bluetooth"
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There is a constant increasing demand for compact, low-cost and low-power portable devices in the world of RF communication transceivers. Due to the continuous progress, high integration capability and low-cost CMOS technology, this research will focus on the design and implementation of RF CMOS power amplifiers since the power amplifier design is a key in the entire RF system. In general, PA's are difficult to integrate in CMOS because of technology limitations (like breakdown voltage) that severely limit the efficiency and linearity of the PA.

This work targets power amplifiers for short-range wireless applications, especially the Bluetooth standard. It first proposes a simple new analytical method using MATLAB for estimating initially the different design parameters incorporated in any stage of the sinusoidal or bias-dependant classes of the CMOS PA design without the blind use of the simulator in the early stage of iterations. The methodology takes into account the effect of the transistor knee voltage. This methodology is compared with simulations using BSIM3v3 transistor model from AMS and it shows a good qualitative agreement and an acceptable quantitative one with the analytical method.

In this thesis also, an overview of the different technology and layout parameters affecting the modeling of the RF MOSFET transistor is presented. The layout-aware macro-model incorporates these parameters in

accordance with the BSIM3v3 compact model is demonstrated and validated by a comparison between simulation results and measurement data - provided by the foundry - for a transistor with total width of 90μm and 18 fingers fabricated using a 0.35μm CMOS process. A Monte-Carlo analysis is performed to explain the slight difference between the measurement and the simulation. This model can be easily modified in order to account for different aspects of the layout unlike the provided model from the foundry.

Finally, a 2.4 GHz power amplifier intended for class 1 Bluetooth applications is designed and implemented using a standard 0.35 μm CMOS process from AMS (Austria Micro Systems). This process has two poly layers, triple metal layers, one thick metal layer, MIM (Metal Insulator Metal) capacitors and high resistive poly module and operates under 3.3 V supply. The design and implementation is done using the RF transistor model. Since the power amplifier design requires lots of simulations iterations even with the use of analytical method to initially estimate its components values, an optimization/synthesis operation based on gradient algorithm optimization is used to speed up the design phase and achieve the required target. This technique strives to find the global minimum of the error function that represents the difference between the achieved specifications and the required ones by finding the slope of this function. After designing the PA, draw its layout and performing the post-layout simulations, the amplifier is capable of delivering a maximum output power of 22 dBm, which is more than required by the Bluetooth standard at the frequency band (2.4 GHz – 2.5 GHz) using a 3.3 V supply. This output power is achieved with an efficiency (η) of 46.1% and an overall power added efficiency (PAE) of 45.5%. The power amplifier employs a class AB in its two stages, which represents a compromise between efficiency and linearity. Thus, it can be easily linearized to satisfy more standards in the

ISM band which utilize non-constant envelope modulation schemes. In addition, it has the power control feature through the use of the bias voltage of a cascode configuration as the control signal. This complies also with the class 1 Bluetooth standard. The designed PA is unconditionally stable in the entire frequency band and achieves a 50Ω input and output matching through the use of on-chip coils except for the choke coil at the drain of the last stage.

Contents

List of Symbols

η	Efficiency
k	Stability factor
Q	Quality factor
PAE	Power Added Efficiency
P_{in}	Input power
P_{out}	Output power
f_o	Required channel frequency
B_1	Required channel bandwidth
B_{adj}	Adjacent channel bandwidth
R_{source}	Source resistance
R_{Lopt}	Optimum load resistance
Ψ	Half conduction angle
ϕ_t	Thermal voltage
ϕ_F	Fermi potential
μ	Carrier mobility
γ	Body effect coeffecient
ε_o	Permittivity of free space
V_{GS}	Gate source voltage
V_{DS}	Drain source voltage
I_d	Drain current
V_T	Threshold voltage
W	Transistor width
L	Transistor length
C'_{ox}	Oxide capacitance per unit area
V_{GB}	Gate bulk voltage
V_{TO}	Zero-bias threshold voltage

V_{SB}	Source bulk voltage
k	Boltzmann constant
q	Electron charge
T	Temperature in kelvin
T_{ox}	Oxide thickness
k_{ox}	Dielectric constant
n_i	Intrinsic electronic concentration
N_a	Substrate doping concentration
ID[0]	Drain current DC component
ID[1]	Drain current fundamental component
ID[2]	Drain current 2^{nd} component
ID[3]	Drain current 3^{rd} component
ID[4]	Drain current 4^{th} component
ID[5]	Drain current 5^{th} component
W_f	Transistor finger width
L_f	Transistor finger length
N_f	Number of fingers
W_{eff}	Transistor effective width
M_i	Intrinsic part of the MOS transistor
Z_{11}	Input impedance
r_p	Polysilicon sheet resistance
r_{cm1p}	Metal1/Poly contact resistance
N_{gc}	Total number of gate contacts
W_g	Polysilicon gate width including the part extending beyond the n^+ diffusion region
$R_{g\text{-}total}$	Overall equivalent gate resistance
g_m	Transconductance
RSH	Diffusion sheet resistance

NRD	Number of squares in the drain region
NRS	Number of squares in the source region
L_d'	Length of the drain diffusion region
L_s'	Length of the source diffusion region
R_{cm1n+}	Contact resistance between M1 and diffusion
C_{jdb}	Drain bulk junction capacitance
C_{jsb}	Source bulk junction capacitance
R_{db}	Drain bulk resistance
R_{sb}	Source bulk resistance
R_{dsb_sh}	Substrate sheet resistance
R_{dsb}	Substrate resistance
$C_{sb,k}$	Source bulk capacitance for each finger
$C_{db,k}$	Drain bulk capacitance for each finger
r_{dbw}	Substrate drain resistance with unit channel width
r_{sbw}	Substrate source resistance with unit channel width
N_{dc}	Number of contacts in the drain region
N_{sc}	Number of contacts in the source region
C_{gso}	Overlap capacitance between gate and source
C_{gdo}	Overlap capacitance between gate and drain
L_{ov}	Overlap between source or drain and gate
D_{db}	Drain bulk diode
D_{sb}	Source bulk diode
$C_{junction}$	Junction capacitance
C_{ja}	Area capacitance of the diffusion region
C_{jswp}	Sidewall capacitance of the diffusion region
AD	Drain area
AS	Source area
PD	Drain perimeter