AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

Design of Low Power CMOS Direct Digital Frequency Synthesizer

A Thesis

Submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

Submitted by

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B.Sc. in Electrical Engineering

(Electronics and Communications Engineering)

Ain Shams University, 2007

Supervised By

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Cairo, 2010

بِسۡمِ ٱللَّهِ ٱلرَّحۡمَٰنِ ٱلرَّحِيمِ

قال الله تعالى:

وَلَٰكِنَّ أَكۡثَرَ ٱلنَّاسِ لَا يَعۡلَمُونَ ٦

يَعۡلَمُونَ ظَٰهِرٗا مِّنَ ٱلۡحَيَوٰةِ ٱلدُّنۡيَا وَهُمۡ عَنِ

ٱلۡأٓخِرَةِ هُمۡ غَٰفِلُونَ ٧

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ٱلْحَمْدُ لِلَّهِ رَبِّ ٱلْعَٰلَمِينَ

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ABSTRACT

Hesham AbdElSalam Omran, Design of Low-Power CMOS Direct Digital Frequency Synthesizer, Master of Science thesis, Ain Shams University, 2010.

In this thesis, the design of low-power direct digital synthesizer is investigated. The continuous down scaling of minimum feature size in CMOS technology allowed whole systems to be implemented on a single chip. These systems incorporate different blocks that require unrelated clock signals with certain frequencies. This raises the need for a frequency synthesis architecture with fine resolution and low-power consumption that can be integrated in modern deep-submicron digital CMOS technologies.

After a brief overview on different frequency synthesis architectures, phase interpolation direct digital synthesizer (DDS) is thoroughly discussed as the main architecture highlighted in the thesis.

An implementation of phase interpolation DDS suitable for FPGA environment is presented. The synthesizer is fully implemented on FPGA and does not require any external analog components, while achieving sub-Hz tuning resolution and sub-μs switching time. Experimental measurements validate system operation with spurious free dynamic range (SFDR) greater than 40 dB.

A DDS-based architecture for jitter-free fractional divider is proposed. Mathematical analysis is provided in addition to simulation results. The design is implemented on FPGA to verify its operation. Measurement results are presented.

An architecture targeted for ASIC implementation is also presented. The design is implemented in 0.13 μm CMOS technology. In addition to being fully monolithic, the design achieves low-power and fine resolution. The design can also be extended to provide multi-channel operation.

Key words: Direct digital synthesizer (DDS), clock generator, fractional divider, phase interpolation, field programmable gate array (FPGA), CMOS, low-power.

SUMMARY

This thesis demonstrates the design of phase interpolation direct digital synthesizer (DDS). The thesis is in **seven** chapters, organized as follows:

Chapter One serves as an introduction. The concept of frequency synthesis is introduced together with the main specifications of a frequency synthesizer. The chapter further illustrates the motivation for the thesis and the thesis outline is presented.

Chapter Two contains a brief overview of different frequency synthesis architectures. The concept of direct and indirect synthesis is introduced. The advantages and disadvantages of each architecture are discussed.

Chapter Three provides a detailed discussion of phase interpolation direct digital synthesizer (DDS), which is the architecture highlighted in this thesis. The idea of operation from both time domain and frequency domain perspectives is presented. A detailed literature survey is then done on different implementation approaches pointing out their pros and cons.

Chapter Four presents an implementation of phase interpolation DDS on FPGA. After a short overview on FPGA technology, the system architecture and blocks are described. Simulation and measurement results in both time domain and frequency domain are discussed.

Chapter Five introduces a DDS-based architecture for a jitter-free fractional divider. The basic idea is illustrated and simulation results are presented. The design is implemented on FPGA and measured in lab.

Chapter Six introduces an ASIC implementation of a phase interpolation DDS in 0.13 μm CMOS technology. The design incorporates a phase locked loop (PLL). Both system and circuit design levels of the PLL are presented. The design of a digital-to-time converter (DTC) is also presented.

Chapter Seven contains final conclusions. The work discussed in this thesis is compared with work published in the literature. Some ideas for future work are then suggested.

Contents

List of Abbreviations and Symbols

A/D Analog-to-digital.

ACC Accumulator.

ASIC Application specific integrated circuit.

ASK Amplitude shift keying.

CAD Computer aided design.

CMOS Complementary metal oxide semiconductor.

CORDIC Co-ordinate rotation digital computer.

D/A Digital-to-analog.

DAC Digital-to-analog converter.

DCM Digital clock manager.

DCVSL Differential cascode voltage switch logic.

DDPS Direct digital period synthesizer.

DDS Direct digital synthesizer.

DLL Delay locked loop.

DPC Digital-to-phase converter.

DSP Digital signal processing.

DTC Digital-to-time converter.

DW Delay word.

ESD Electrostatic discharge.

FB Feed-back.

FCW Frequency control word.

FF Feed-forward.
Flip-flop.

FOM Figure of merit.

FPGA Field programmable gate array.

FSK Frequency shift keying.

HDL-AMS Hardware description language - analog/mixed signal.

IC Integrated circuit.

INC Increment.

LPF Low pass filter.

LUT Look-up table.

NA Not available.

NCO Numerically controlled oscillator.

PD Phase detector.

PFD	Phase-frequency detector.
PINC	Phase increment.
PLL	Phase locked loop.
PSK	Phase shift keying.
PVT	Process, voltage, and temperature.
RF	Radio frequency.
ROM	Read-only memory.
S/H	Sample and hold.
SFDR	Spurious free dynamic range.
SNR	Signal to noise ratio.
SoC	System-on-a-chip.
SR	Spur reduction.
VCO	Voltage controlled oscillator.
ZOH	Zero-order hold.
—	—
α^2	PLL loop filter pole-to-zero ratio.
Δf	Frequency step (resolution) (Hz).
ω_n	Second order system natural frequency (rad/s).
ω_{ref}	Reference frequency (rad/s).
ω_u	Unity gain frequency (cross-over frequency) (rad/s).
ϕ_m	Phase margin (degree).