AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
CAIRO - EGYPT

Electronics and Communications Engineering Department

Low Power Arithmetic Unit for 3D Graphics Applications

A thesis submitted in partial fulfilment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

By

Dina Mohamed Mahmoud Ellaithy
Research Assistant at Microelectronics Department
Electronics Research Institute, Giza, Egypt.
Supervised By

Prof. Abdelhalim Abdelnaby Zekry
Ain Shams University, Cairo, Egypt.

Prof. Amal Zaki Mohamed
Electronics Research Institute, Giza, Egypt.

Assoc. Prof. Magdy Ali Elmoursy
Electronics Research Institute, Giza, Egypt.

Cairo 2018

AIN SHAMS UNIVERSITY
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Examiners Committee

Name: Dina Mohamed Mahmoud Ellaithy

Thesis: Low Power Arithmetic Unit for 3D Graphics Applications

Degree: Doctor of Philosophy in Electrical Engineering (Electronics and Communications Engineering)

Title, Name, and Affiliation **Signature**

1. **Prof. Yehea Ismail Mohamed Kamel** ……

Faculty of Engineering - The American University in Cairo.

2. **Prof. Mohamed Amin Ebrahim Dessouky** ……

Faculty of Engineering - Ain Shams University.

3. **Prof. Abdelhalim Abdelnaby Zekry** ……

Faculty of Engineering - Ain Shams University

4. **Prof. Amal Zaki Mohamed** ……

Microelectronics Dept. - Electronics Research Institute

Date: / / 2018

Statement of Original Authorship

This thesis is submitted as a partial fulfilment of Doctor of Philosophy degree in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Name: Dina Mohamed Mahmoud Ellaithy

Signature:

Date : / / 2018

Researcher Data

Name : Dina Mohamed Mahmoud Ellaithy.

Date of birth : 05 November 1983.

Place of birth : Cairo.

Last academic degree : Master of Science in Electrical Engineering

Field of specialization : Electronics and Communications Engineering.

University issued the degree: Ain Shams University.

Date of issued degree : May 2013.

Current job : Research Assistant, Electronics Research Institute.

Acknowledgment

All my thanks to Allah for the successful completion of this work. I express my deepest gratitude and thanks to **Prof. Abdelhalim Zekry**, Ain Shams University, for his continuous supervision support. **Prof. Zekry** is behind all analytical, technical and even spiritual actions throughout this work.

Also, my deepest gratitude and thanks to **Prof. Magdy Elmoursy**, Mentor Graphics, for his outstanding support, patience, encouragement, and continuous guidance without which this thesis would have never been completed. He has been source of ideas and knowledge, yet, his wisdom allowed me to direct my research successfully. I would like to express my gratitude for his great availability and scientific support.

Special thanks to **Prof. Amal Zaki**, Electronics Research Institute, for her constant help and support along the way of my work.

Also, special thanks and appreciation to **Dr. Ghada Hamdy**, Electronics Research Institute, for her interest and valuable assistance.

I would also like to thank my examination committee members: **Prof. Yehea Ismail** and **Prof. Mohamed Dessouky,** thanks to you for serving as my committee members.

I also thank my colleagues at the Electronic Research Institute. Our discussions and meetings allowed me to improve my work. I wish them continued success in their careers.

Many thanks to my mother, father, and brothers for their great hearts which looked after me all these years and always encourages me for further progress.

Dina Mohamed Mahmoud Ellaithy

Abstract

Graphical processing units (GPUs) have wide variety of applications in different fields such as compute art, engineering, science, medicine, entertainment, advertising, visualization, military, and graphical user interface. The growth in the GPUs applications has led to evolution in the hardware design to handle the needed increase in performance. Also, the fast growth of the mobile electronics market and the transition from text based applications to versatile multimedia applications resulted in increasing the popularity of mobile communication devices. Real-time 3D graphics are becoming one of the greatest interesting applications in mobile workstations due to their benefits for gaming, advertising, marketing, and avatar. GPUs are mainly composed of several unified shaders. Each unified shader contains general purpose arithmetic unit and special function units (SFUs) that are used for computing special transcendental and algebraic functions not provided by the general function unit. Functions such as sine, cosine, reciprocal, logarithm, exponential, and compound functions are computed by SFUs. These functions use most of the clock cycles in the real time 3D graphics systems. As a result of that, they consume most of the computing power. Accordingly, reducing the power consumption of the arithmetic unit inside the programmable shaders is the main target for the optimization effort.

An energy efficient Double Logarithmic Arithmetic (DLA) technique is proposed for 3D graphics applications. DLA manipulates the logarithmic arithmetic and improves the architecture for the realization of the transcendental functions and the advanced lighting model using energy efficient techniques. The DLA features complete elimination of multipliers in logarithmic domain by using successive logarithmic converters. This work demonstrates up to 56% reduction in power consumption as compared to the existing techniques. The main advantage of this approach is the ability to perform the complex functions using power-efficient, area-efficient, as well as high frequency design. The proposed technique performs transcendental functions using the multiplier free hardware architecture. Moreover, based on non-uniform subdivisions and piecewise linear approximation, novel logarithmic and antilogarithmic converters are also proposed. These converters achieve optimal power consumption as compared to several recent approaches. They provide low relative error with less non-uniform subdivisions. Up to 19%, 12%, and 20% reduction in relative error, area, and power consumption, are achieved, respectively.

In addition, a dual channel multiplier (DCM) for energy efficient second order piecewise-polynomial function evaluation for 3D graphics applications is proposed. The performance of the evaluation process is highly dependent on the design of the multiplication and squaring structure.

A novel hardware implementation for polynomial evaluation is presented. The proposed approach compensates the complex multipliers by using DCM which reduces the hardware complexity. The DCM scheme performs complex functions with power-efficient and area-efficient approaches. The multiplier reduces the hardware computational effort in the piecewise polynomial approximation with uniform or non-uniform segmentation. For large operand input size, multiplier adder converter (MAC) and a dedicated radix4 squaring unit are also proposed. These units achieve the least power consumption as compared to previous approaches with large input word size. Comparison with general-purpose multiplication has shown reduction in power, and delay by up to 36%, and 50%, respectively. The proposed technique exhibits up to 93% saving in power consumption as compared to the current traditional schemes. This thesis presents novel designs of low power and low complexity arithmetic unit for GPU. The proposed arithmetic units suitable for low-power 3D graphics applications.

Keyword: antilogarithmic converter, double logarithmic arithmetic (DLA) unit, graphical processing unit (GPU), logarithmic arithmetic unit, logarithmic converter, low power.

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