AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Department

Design of Wireless Transceiver Front-end

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Ahmed Mohamed Attia Zamzam

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2012

Supervised By

Prof. Hani Fikry Ragai

Dr. Mohamed Ahmed Mohamed El - Nozahi

Cairo – (2018)

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Date: 25 July 2018

Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain Shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

There is a huge demand for fully integrated, small size, and highly efficient transceivers, due to the enormous growth of wireless applications. Power amplifier (PA), specifically determines the performance of these transceivers, as it is the most power hungry block. Hence, any enhancement in its efficiency would result in a great decrease in the total power consumption. This thesis aims to study the technology performance limits as well as the design challenges of PAs. Due to the fact that the transceivers need to not only support high data rates but also have small cost, the main focus is on the commercial low cost CMOS technologies. Different active and passive loss mechanisms have been studied, and a new cascode switching technique has been proposed to increase the efficiency at 15 GHz. The proposed technique results in an enhancement of PAE by about 10.6 %.

In the recent years, a huge attention has been drawn to millimetre frequency range. This can be explained by the huge bandwidth allocated in these bands, which can result in very high data rates. In addition, the high frequency design enables the implementation of small size and high quality passives, which helps in achieving low cost, small form factor transceivers. 60 GHz offers an additional advantage, which is the reduced coverage range, and this provides better security. A state of the art ON/OFF key (OOK) 60 GHz transceiver architecture has been proposed. This architecture enables delivering high output power and low noise figure. In addition, a 60 GHz transmitter has been designed in bulk 65nm CMOS process. The transmitter utilizes a new current combined stacked injection locking topology which enhances both output power and efficiency. This PA delivers 19.5dBm output power with 15.5 % PAE.

The transmitter occupies an area of 1.5mmx1.2mm. Modelling of all the implemented inductors, capacitors as well as the layout routings is carried out using the electromagnetic simulator, SONNET. Post layout simulations show that the transmitter can deliver 20dBm output power with 10 % efficiency.

Thesis Summary

The thesis is divided to six chapters as listed below,

Chapter 1

In this chapter, an introduction about the design of CMOS transceivers is presented. Then the objectives of the thesis, as well as its contributions are demonstrated. Finally, the organization of the thesis is briefly discussed.

Chapter 2

Chapter 2 gives a sufficient background of different transmitter architectures, with a bigger focus on PAs. Several classes of PAs are demonstrated, and in addition, a survey of the existing techniques to enhance its performance is provided. Finally, the design challenges and the loss mechanisms of Class E PAs are studied, and the technology performance limits are highlighted.

Chapter 3*

In Chapter 3, the drawbacks of the conventional methodology of stacked PAs are demonstrated. A new cascode switching technique is proposed in order to mitigate the loss caused by these drawbacks. The theory is carried to design a PA at 15 GHz using 0.13u CMOS technology. A comparison is performed with a classic double stacked design. Simulation results show enhancement in both output power and power added efficiency by about 9% and 10.6% respectively.

* The cascode enhancement technique was accepted for publication in 61st IEEE International Midwest Symposium on Circuits and Systems (2018)

Chapter 4*

In Chapter 4, A Current combined, stacked, injection locking technique is proposed in order to enhance both output power and power-added efficiency (*PAE*). Based on this introduced technique, a 60 GHz fully differential stacked power amplifier is designed in 65nm CMOS bulk process. The simulation results show an output power of 19.5dBm and *PAE* of 15.5%. Worst case process corners simulations are also provided.

Chapter 5

Chapter 5 focuses on the system level design of the front end of an OOK 60 GHz transceiver. A complete set of system specifications are provided using the link budget equations. In addition, the design of an up-conversion mixer, a power amplifier, a balun and a power combiner is demonstrated. Finally, post layout simulations of the transmitter are shown.

Chapter 6

In chapter 6, the thesis is summarized where the main contributions are highlighted. In addition, possible future research directions are suggested.

Keywords: 60GHz transmitter, 60GHz power amplifier, injection locking, cascode switching, Wilkinson power combiner.

* The 60 GHz stacked injection locking power amplifier was published in the 19th annual IEEE Wireless and Microwave Technology Conference (WAMICON 2018).

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Ahmed Mohamed Attia Zamzam

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