AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Time-Domain Sensing for Non-Volatile Memories

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by

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Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2012

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Dr. Ihab Adly

Cairo, 2018

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electronics Engineering and Electrical Communications, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

A fast sense amplifier (SA) with high resolution is required to face the challenges of sensing techniques in embedded memory systems in micro-controller units (MCU's). Robustness, speed, area of the SA impact the performance of integrated memories in many applications of the automotive industry (electric and hybrid vehicles). Also, improving the sensing technique of the SA reduces the access time of embedded flash memories. As a result, automotive applications including car safety, comfort electronics, and system security performance are enhanced.

The motivation of this work is to present, compare and analyse performance parameters of time-continuous sense amplifiers for time sensing techniques within non-volatile flash memories. Key benchmark parameters impacting the performance of the comparator design of the SA are speed, gain, offset, power consumption and resolution. Firstly, these variables were reviewed and compared analytically within state-of-the-art sense amplifier designs. The latest memory sensing research [1] [2] considers the common gate SA approach to deliver the highest performance in the market with 65nm and 28nm technologies. To date, the performance of differential based approach has not been compared to common gate approach using 28nm technology for time sensing techniques.

Secondly, circuit design and simulation results of a time domain sense amplifier based on differential pair approach for multi-level-cell (MLC) embedded memories are presented in 28nm technology. This SA design provides lower sensing delay and higher selectivity for stronger programmed cells compared to the state-of-the-art common gate approach in automotive SA designs when simulated in 28nm technology [3]. Moreover, additional benefits including offset cancellation, high gain and resolution were achieved.

The work is organised as follows. In Chapter 1, an overview of the flash memory cell basic structure and different sensing techniques will be provided. The advantages of time-domain sensing in addition to market-leading time-continuous sense amplifier designs which is the focus of this work will be presented. In Chapter 2, comparative analysis at the system level is undertaken for market-leading sense amplifier designs in time domain sensing. The relative delay and power consumption of the state-of-the-art SA are compared in 65 and 28 nm technologies. The differential pair approach is identified as having a higher potential for lower delay in comparison to the common gate approach in small node 28nm technologies. Chapter 3 outlines design specifications for a differential pair based sense amplifier with offset cancellation technique for robust and reliable SA in 28nm technology.

Chapter 4 describes the methodology for testing the performance of differential pair approach designed in Chapter 3. Firstly, MLC concept, application environment

and its biasing techniques are described. The simulation results of the time domain sensing design in 28nm technology are then presented when applying various sense voltage and bit line capacitance. Results indicate that the proposed differential pair based SA operates at high performance with low sense voltage and high bit line capacitance.

Chapter 5 builds on the performance evaluation of the differential pair SA design by adding in comparative simulations between the state-of-the-art common gate sense amplifiers and the proposed sense amplifier in terms of power consumption, selectivity for stronger programmed cells and propagation delay in 28nm technology. The proposed differential based SA design is superior to the state-of-the-art common gate sense amplifiers in terms of delay time with the advantage of high selectivity for stronger programmed cell at the cost of higher power consumption. Th figure of merit of the high performance differential based SA is comparable to that of the common gate based SA.

Finally, Chapter 6 explores future implications of a fast and low power sense amplifiers with the challenges in the automotive industry facing the embedded memories. A brief overview of automotive functional safety security standard ISO62622 with a focus on difficulties facing sense amplifies is presented. Moreover, relative importance of design trade-offs for future designs research of SA using time sensing approaches within the automotive industry are given.

keywords: embedded flash, multi-level flash, sense amplifier, 28 nm, time domain sensing

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Abbreviations and Symbols

ADAS	advanced driver assistance systems
C_{BL}	bit line capacitance
CHE	channel hot electrons injection
C_{load}	the load capacitance
FN	Fowler-Nordheim
FOM	figure of merit
GBL	global bit line
I_{bias}	biase current
I_{ds}	transistor saturation current
I_{read}	read current
ISO62622	standard for speed and security for automotive applications
LBL	local bit line
MCU's	micro-controllersunits
MLC	multi-level-cell
MONOS	metal-oxide-nitride-oxide-silicon
MUX	multiplexer
OEM	Original-Equipment-Manufacturers
$P_{Ctt,65nm}$	the power consumption of the common gate approach
$P_{limit,tech}$	the minimum power consumption fo this technology
R_{BL}	bit line resistance
SA	sense amplifer
SG	split gate
SLC	single-level-cell
t_{acc}	access time of sensing
t_{Cha}	charging time needed for the accumulated charge on the C_{BL} to reach V_{sense}
t_{Cha}	charging time of the bit line capacitor to V_{sense}
$t_{CompDelay}$	the delay time of the comparator
$t_{precharge}$	precharge time to reset the bit line voltage
t_{ref}	reference time
t_{sense}	sensing time
$t_{trig,MatrixCell}$	trigger time of matrix cell
t_1	time at output ONE
t_0	time at output ZERO
V_{BL}	bit line voltage
V_{Ctt}	control gate voltage
V_{DD}	supply voltage
V_g	voltage at the gate of the transistor

V_{pre}	precharge voltage
V_{read}	read voltage
V_{ref}	reference voltage
v_{sense}	sense voltage
V_{ss}	ground voltage
$V_{th,shifted}$	shifted threshold voltage
V_{thj1j}	threshold voltage for logic ONE
V_{thj0j}	threshold voltage for logic ZERO
V_{out}	output voltage
V_{ov}	overdrive voltage
V_0	Output voltage of ZERO
V_1	Output voltage of ONE

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