



DYNAMIC PARTIAL RECONFIGURATION VERIFICATION AND APPLICATIONS ON FPGA **DEBUGGING**

By

Islam Osama Ahmed Mounir Mostafa

A Thesis Submitted to the Faculty of Engineering at Cairo University in Partial Fulfillment of the Requirements for the Degree of MASTER OF SCIENCE

in

Electronics and Electrical Communications Engineering

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FACULTY OF ENGINEERING, CAIRO UNIVERSITY GIZA, EGYPT 2018

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| • | ration (DPR); Verification mmable Gate Arrays (FPG | | |
| Summary: | | | |
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Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

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