AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Computer and Systems Engineering Department

Thread Migration Optimization for Chip Multiprocessors

A Thesis submitted in partial fulfillment of the requirements of
Master's Degree in Electrical Engineering
(Computer and Systems Engineering)

by
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Bachelor of Science in Electrical Engineering
(Computer and Systems Engineering Department)
Faculty of Engineering, Ain Shams University, 2013

Supervised By
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Cairo, 2018

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Date:29 September 2018

Statement

This thesis is submitted as a partial fulfillment of Master's Degree in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Date: 29 September 2018

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Thesis Summary

This thesis presents an efficient heuristic for dynamically assigning threads to system cores such that performance requirements are met while minimizing the energy consumed. The heuristic can be applied to heterogeneous systems and homogeneous systems with DVFS capabilities.

Summary

The thesis is divided into seven chapters as listed below:

Chapter 1 is an introduction to this research. This chapter provides an overview about the problem of thread assignment under performance constraints, the hardware systems considered in the scope of this research and the potential applications of our proposed method.

Chapter 2 provides the necessary background and explores recently-proposed related research work. Three main approaches for dealing with systems with power or performance constraints are discussed. Some studies propose algorithms to address the thread scheduling problem on heterogeneous multi-core systems. Others address power constraints using DVFS. Finally, several research studies propose reconfigurable architectures to deal with program variations and constraints. We discuss recent proposals for these three approaches and highlight the use cases for each one as well as the systems most suitable for utilizing these methods.

Chapter 3 describes the proposed thread mapping framework. The formulation of the thread mapping problem, the system model used in this work and the proposed heuristic solution are shown. Furthermore, this chapter describes the means of applying our solution to systems with heterogeneous cores and systems with homogeneous cores with DVFS capabilities. Applying the proposed solution to two different schemes of DVFS algorithms for homogeneous chips and the benefits of each is also detailed in this chapter.

Chapter 4 shows the implementation details of the proposed framework. The prediction method utilized for estimation of power and performance values is presented, together with the associated prediction error percentage. Moreover, the data structures used in the implementation of the algorithm, to ensure that it can be brought online for hundred-core systems with minimal overhead, are described.

Chapter 5 shows the experimental setup used to conduct simulations and tests. The different systems used for testing are described, along with their various configurations. A

background about the architectural simulator used for testing and the reason for choosing this specific tool is provided. Additionally, the benchmarks used in the simulations and their input sets are described.

Chapter 6 presents the experimental results from the simulations and an evaluation of the proposed framework. Comparisons are conducted between the results obtained for the different systems we tested our framework on as well as comparison with a recently-proposed thread scheduling heuristic. The scalability and complexity of the proposed algorithm are also evaluated.

Chapter 7 concludes this thesis. The most significant results of this work are summarized and directions for future work are provided.

Key words: dynamic scheduling, optimization, dynamic voltage/frequency scaling (DVFS), heterogeneous many-core, performance constraints, low-power

Abstract

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Thesis title: **Thread Migration Optimization for Chip Multiprocessors**
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Abstract

Efficiently mapping threads to system cores is critical for achieving high performance and power efficiency in multicore systems. Conventional scheduling techniques do not take system heterogeneity and varying DVFS states into account and therefore do not produce efficient mappings. Additionally, since thread behavior varies throughout its execution, a fixed thread-to-core mapping is suboptimal. Dynamically scheduling threads to appropriate core states can significantly improve system throughput and decrease energy consumption. Scheduling decisions are of utmost importance in systems that have performance constraints to satisfy. The problem of thread assignment in order to meet performance or power constraints has been shown to be NP-complete and therefore exceedingly expensive to solve online. This thesis proposes an efficient heuristic for dynamically assigning threads to system cores such that performance requirements are met while minimizing the energy consumed. The heuristic can be applied to heterogeneous systems and homogeneous systems with DVFS capabilities. Simulation results show that the heuristic can be used online in hundred-core systems, with runtime overhead of less than 1 millisecond for 256-core systems.

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