HARDWARE IMPLEMENTATION OF SOFTWARE DEFINED RADIO BASED ON DYNAMIC PARTIAL RECONFIGURATION

By

Sherif Mohamed Hosny Afifi

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

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Title of Thesis:

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Key Words:
Software Defined Radio; Dynamic Partial Reconfiguration; Field Programmable Gate Array

Summary:

This work implements SDR transceiver system for five wireless communication standards: Bluetooth, Wi-Fi, 2G, 3G, and LTE on Zynq-7000 evaluation kit. The new DPR technique is used to switch between different multi-standard communication systems on the same FPGA partition. Implementing SDR using DPR combines the advantage of hardware performance and software flexibility. A test environment is established to measure the effectiveness of the new technique.

Disclaimer

I herby declare that this thesis is my own original work, and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately ackowleged al sources used have cited them in the refernces section.

Name:

Signature:

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List of Nomenclature

Abbreviation	Description
2G	Second Mobile Generation.
3G	Third Mobile Generation.
3GPP	3rd Generation Partnership Project.
ADC	Analog to Digital Converter.
ASIC	Application Specific Integrated Circuit.
AXI	Advanced Extensible Interface.
BPSK	Binary Phase Shift Keying.
BRAM	Block Read Access Memory.
CDMA	Code Division Multiple Access.
CRC	Cyclic Redundancy Check.
DAC	Digital to Analog Converter.
DDR	Double Data Rate.
DPR	Dynamic Partial Reconfiguration.
DSP	Digital Signal Processing.
FEC	Forward Error Correction.
FIFO	First Input First Output.
FPGA	Field Programming Gate Array.
FSM	Finite State Machine.
GPP	General Purpose Processor.
HDL	Hardware Description Language.
GSM	Global System for Mobile communications.
ICAP	Internal Configuration Access Port.
IFFT	Inverse Fast Fourier Transform.
IEEE	Institute of Electrical and Electronic Engineers.
ILA	Interactive Logic Analyzer.
JTAG	Joint Test Action Group.
LTE	Long Term Evolution.
LUT	Look Up Table.
OFDM	Orthogonal Frequency Division Multiplexing.
PL	Programmable Logic.
PRC	Partial Reconfiguration Controller.
PS	Processing System.
PLB	Programmable Logic Block.
RM	Reconfigurable Module.
RP	Reconfigurable Partition.

QAM	Quadrature Amplitude Modulation.
QPSK	Quadrature Shift Keying.
SCFDMA	Single Carrier Frequency Division Multiple Access.
SDK	Software Development Kit.
SDR	Software Defined Radio.
SoC	System on Chip.
TTI	Transmission Time Interval.
SRAM	Static Random Access Memory.
UMTS	Universal Mobile Telecommunications System.

Abstract

Dynamic Partial Reconfiguration (DPR) has been used extensively over the past few years allowing reconfiguration of Field Programmable Gate Arrays (FPGAs) during the run time. FPGA is considered one of the best solutions for implementing reconfigurable hardware. The concept of hardware reconfiguration exists for several decades and passed through many evolution phases. With the aid of DPR, multi-standard Software Defined Radio (SDR) system can be implemented in order to save power and area extensively. Over the past few years, wireless communication standards witnessed great and rapid evolution. The market is always acquiring higher data rates and more special services. This leads to increasing the design complexity, area, and power consumption. Deploying DPR technology on FPGAs made it feasible to design and manufacture all wireless communications standards on the same hardware. Loading each standard on demand reduces area utilization and power consumption.

SDR is a communication system whose physical layer is used to do all the computations using the software. The communication blocks in ordinary radio transceivers are designed in a fixed environment to process a certain waveform. SDR is able to process many waveforms since it can be easily configured using software. It is becoming achievable, as the flexibility in the digital front-end reconfiguration increases. One of the advantages of implementing the SDR is increasing the flexiblity that aids in performing dynamic and real-time reconfiguration. Another advantage of using SDR is the efficient use of resources under varying conditions. Bottom line is, the hardware flexibility allows the SDR dynamic system to implement different standards within real-time without the need to switch off the system. The fundamental challenge facing the deployment of SDR is how to achieve sufficient computational capacity, in particular for processing wide-band high bit rate waveforms, within acceptable size and weight factors, within acceptable unit costs, and reduced power consumption compared to the communication standards implemented in current mobile phones.

This work implements SDR transceiver system for five wireless communication standards: Bluetooth, Wi-Fi, 2G, 3G, and LTE on Zynq-7000 evaluation kit. The new DPR technique is used to switch between different multi-standard communication systems on the same FPGA partition. Implementing SDR using DPR combines the advantage of hardware performance and software flexibility. A test environment is established to measure the effectiveness of the new technique. Two approaches are deployed to implement the five transceivers using DPR. The first technique uses a single reconfigurable partition for the transmitter and the receiver. The second technique recommends splitting the design into multi-partitions in order to achieve the best performance for all transceivers. A comparison is performed for the system total area and power consumption between the two DPR approaches and the case of no DPR. The single partition approach achieves reduction of area and power by 10.19% and 76.71% respectively with a reasonable switching time. The multi-partition approach is able to reduce the allocated area and power consumption for all chains. Power reduction for 2G and Bluetooth is 95.43%, for 3G and Wi-Fi is 79.69%, for LTE is 59.09% compared with the case of no DPR.