



Cairo University

# **HARDWARE IMPLEMENTATION OF SOFTWARE DEFINED RADIO BASED ON DYNAMIC PARTIAL RECONFIGURATION**

By

**Sherif Mohamed Hosny Afifi**

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
in Partial Fulfillment of the  
Requirements for the Degree of  
**MASTER OF SCIENCE**  
in  
**Electronics and Communications Engineering**

FACULTY OF ENGINEERING, CAIRO UNIVERSITY  
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Under the Supervision of

**Prof. Dr. Ahmed H. Khalil**

**Dr. Hassan Mostafa Hassan**

Professor  
Electronics and Electrical Communications  
Engineering Department  
Faculty of Engineering, Cairo University

Assistant Professor  
Electronics and Electrical Communications  
Engineering Department  
Faculty of Engineering, Cairo University

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Approved by the  
Examining Committee

---

**Prof. Dr. Ahmed H. Khalil**

Thesis Main Advisor

---

**Prof. Dr. Mohamed F. Abu-ElYazeed**

Internal Examiner

---

**Dr. Magdy A. El-Moursy**  
(Electronics Research Institute)

External Examiner

FACULTY OF ENGINEERING, CAIRO UNIVERSITY  
GIZA, EGYPT  
2018

**Engineer's Name:** Sherif Mohamed Hosny Afifi  
**Date of Birth:** 15/2/1993  
**Nationality:** Egyptian  
**E-mail:** [Sherif1521993@gmail.com](mailto:Sherif1521993@gmail.com)  
**Phone:** 01005264022  
**Address:** 39 El-Maraghi street, El-Agouza  
**Registration Date:** 1/3/2015  
**Awarding Date:** 2018  
**Degree:** Master of Science  
**Department:** Electronics and Communications Engineering



**Supervisors:**

Prof. Dr. Ahmed H. Khalil  
Dr. Hassan Mostafa Hassan

**Examiners:**

Prof. Dr. Ahmed H. Khalil (Thesis Main Advisor)  
Prof. Dr. Mohamed F. Abu-ElYazeed (Internal Examiner)  
Dr. Magdy A. El-Moursy (External Examiner)  
(Electronics Research Institute)

**Title of Thesis:**

HARDWARE IMPLEMENTATION OF SOFTWARE DEFINED RADIO BASED  
ON DYNAMIC PARTIAL RECONFIGURATION

**Key Words:**

Software Defined Radio; Dynamic Partial Reconfiguration; Field Programmable Gate Array

**Summary:**

This work implements SDR transceiver system for five wireless communication standards: Bluetooth, Wi-Fi, 2G, 3G, and LTE on Zynq-7000 evaluation kit. The new DPR technique is used to switch between different multi-standard communication systems on the same FPGA partition. Implementing SDR using DPR combines the advantage of hardware performance and software flexibility. A test environment is established to measure the effectiveness of the new technique.

# Disclaimer

I hereby declare that this thesis is my own original work, and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name:

Signature:

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# List of Nomenclature

<b>Abbreviation</b>	<b>Description</b>
<b>2G</b>	Second Mobile Generation.
<b>3G</b>	Third Mobile Generation.
<b>3GPP</b>	3rd Generation Partnership Project.
<b>ADC</b>	Analog to Digital Converter.
<b>ASIC</b>	Application Specific Integrated Circuit.
<b>AXI</b>	Advanced Extensible Interface.
<b>BPSK</b>	Binary Phase Shift Keying.
<b>BRAM</b>	Block Read Access Memory.
<b>CDMA</b>	Code Division Multiple Access.
<b>CRC</b>	Cyclic Redundancy Check.
<b>DAC</b>	Digital to Analog Converter.
<b>DDR</b>	Double Data Rate.
<b>DPR</b>	Dynamic Partial Reconfiguration.
<b>DSP</b>	Digital Signal Processing.
<b>FEC</b>	Forward Error Correction.
<b>FIFO</b>	First Input First Output.
<b>FPGA</b>	Field Programming Gate Array.
<b>FSM</b>	Finite State Machine.
<b>GPP</b>	General Purpose Processor.
<b>HDL</b>	Hardware Description Language.
<b>GSM</b>	Global System for Mobile communications.
<b>ICAP</b>	Internal Configuration Access Port.
<b>IFFT</b>	Inverse Fast Fourier Transform.
<b>IEEE</b>	Institute of Electrical and Electronic Engineers.
<b>ILA</b>	Interactive Logic Analyzer.
<b>JTAG</b>	Joint Test Action Group.
<b>LTE</b>	Long Term Evolution.
<b>LUT</b>	Look Up Table.
<b>OFDM</b>	Orthogonal Frequency Division Multiplexing.
<b>PL</b>	Programmable Logic.
<b>PRC</b>	Partial Reconfiguration Controller.
<b>PS</b>	Processing System.
<b>PLB</b>	Programmable Logic Block.
<b>RM</b>	Reconfigurable Module.
<b>RP</b>	Reconfigurable Partition.

<b>QAM</b>	Quadrature Amplitude Modulation.
<b>QPSK</b>	Quadrature Shift Keying.
<b>SCFDMA</b>	Single Carrier Frequency Division Multiple Access.
<b>SDK</b>	Software Development Kit.
<b>SDR</b>	Software Defined Radio.
<b>SoC</b>	System on Chip.
<b>TTI</b>	Transmission Time Interval.
<b>SRAM</b>	Static Random Access Memory.
<b>UMTS</b>	Universal Mobile Telecommunications System.

# Abstract

Dynamic Partial Reconfiguration (DPR) has been used extensively over the past few years allowing reconfiguration of Field Programmable Gate Arrays (FPGAs) during the run time. FPGA is considered one of the best solutions for implementing reconfigurable hardware. The concept of hardware reconfiguration exists for several decades and passed through many evolution phases. With the aid of DPR, multi-standard Software Defined Radio (SDR) system can be implemented in order to save power and area extensively. Over the past few years, wireless communication standards witnessed great and rapid evolution. The market is always acquiring higher data rates and more special services. This leads to increasing the design complexity, area, and power consumption. Deploying DPR technology on FPGAs made it feasible to design and manufacture all wireless communications standards on the same hardware. Loading each standard on demand reduces area utilization and power consumption.

SDR is a communication system whose physical layer is used to do all the computations using the software. The communication blocks in ordinary radio transceivers are designed in a fixed environment to process a certain waveform. SDR is able to process many waveforms since it can be easily configured using software. It is becoming achievable, as the flexibility in the digital front-end reconfiguration increases. One of the advantages of implementing the SDR is increasing the flexibility that aids in performing dynamic and real-time reconfiguration. Another advantage of using SDR is the efficient use of resources under varying conditions. Bottom line is, the hardware flexibility allows the SDR dynamic system to implement different standards within real-time without the need to switch off the system. The fundamental challenge facing the deployment of SDR is how to achieve sufficient computational capacity, in particular for processing wide-band high bit rate waveforms, within acceptable size and weight factors, within acceptable unit costs, and reduced power consumption compared to the communication standards implemented in current mobile phones.

This work implements SDR transceiver system for five wireless communication standards: Bluetooth, Wi-Fi, 2G, 3G, and LTE on Zynq-7000 evaluation kit. The new DPR technique is used to switch between different multi-standard communication systems on the same FPGA partition. Implementing SDR using DPR combines the advantage of hardware performance and software flexibility. A test environment is established to measure the effectiveness of the new technique. Two approaches are deployed to implement the five transceivers using DPR. The first technique uses a single reconfigurable partition for the transmitter and the receiver. The second technique recommends splitting the design into multi-partitions in order to achieve the best performance for all transceivers. A comparison is performed for the system total area and power consumption between the two DPR approaches and the case of no DPR. The single partition approach achieves reduction of area and power by 10.19% and 76.71% respectively with a reasonable switching time. The multi-partition approach is able to reduce the allocated area and power consumption for all chains. Power reduction for 2G and Bluetooth is 95.43%, for 3G and Wi-Fi is 79.69%, for LTE is 59.09% compared with the case of no DPR.