



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

**Electronics Engineering and Electrical Communications
Department**

Low Voltage Static Random Access Memory

A Thesis submitted in partial fulfillment of the requirements of
Master of Science degree in Electrical Engineering
Electronics Engineering and Electrical Communications Department

By

Reem Sherif El Senousy Mohamed

Bachelor of Science degree in Electrical Engineering Electronics Engineering and Electrical
Communications Department
Faculty of Engineering, Ain shams University, 2012

Supervised By

Prof. Dr. Wagdy Refaat Anis

Dr. Sameh Assem Ibrahim

Cairo, 2018



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Electrical Communications Engineering

Low Voltage Static Random Access Memory

by

Reem Sherif EL Senousy Mohamed

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2012

Examiners' Committee

Name and Affiliation

Signature

Prof. El-Sayed Mostafa Saad

Electronics & Communications Dept.
Faculty of Engineering, Helwan University

.....

Prof. Mohamed Amin Dessouky

Electronics & Communications Dept.
Faculty of Engineering, Ain Shams University

.....

Prof. Wagdy Refaat Anis

Electronics & Communications Dept.
Faculty of Engineering, Ain Shams University

.....

Date: 20 September 2018

Statement

This thesis is submitted as a partial fulfillment of Master of Science degree in Electrical Engineering, Faculty of Engineering, Ain Shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Reem Sherif El Senousy Mohamed

Signature

.....

Date: 20 September 2018

Researcher Data

Name: Reem Sherif EL Senousy Mohamed

Date of Birth: 18/07/1990

Place of Birth: Cairo, Egypt

Last academic degree: B.Sc. in Electrical Engineering

Field of specialization: Electronics Engineering and Electrical Communications Department

University issued the degree: Ain Shams University

Date of issued Degree: 2012

Current job: Graduate Student at Ain Shams University

**Faculty of Engineering - Ain Shams University Electronics and
Communication Engineering Department**

Thesis title:” Low Voltage Static Random Access Memory”

Submitted by: Reem Sherif El Senousy Mohamed

Degree: Master of Science in Electrical Engineering

Summary

Recently, with the move towards very-low power applications, Static Random Access Memories (SRAMs) are operated at very-low supply voltages to reduce their power consumption. As a result, speed is affected, and data reliability becomes more vulnerable to noise imposing strict constraints on 6 Transistors (6T) SRAM cell design. This work focuses on 6T SRAM cell noise margin and access time analysis and modeling in addition to a new optimization methodology. The thesis consists of seven chapters including lists of contents, tables and figures as well as list of references and three appendices.

Chapter 1: contains thesis introduction, as well as literature review.

Chapter 2: presents memory background. It focuses on the SRAM architecture at the system and the bit cell level. Moreover, it shows SRAM different modes of operation including a comparison between SRAM bit cell designs at weak and strong inversion regions using 65nm CMOS technology.

Chapter 3: discusses and evaluates SRAM essential performance metrics; noise margin, access time, power and leakage. As well as the tradeoffs between these parameters facing the SRAM designer at Ultra low voltage cell design.

Chapter 4: includes analytical modeling for SRAM noise margin

for different modes using state space equation at sub threshold region.

Chapter 5: timing analysis for read and write operations at sub threshold region are discussed.

Chapter 6: explores the new proposed optimal design methodologies

Chapter 7: presents the thesis conclusion and some suggested future work.

Abstract

**Faculty of Engineering - Ain Shams University
Electronics and Communication Engineering Department**

Thesis title:” **Low Voltage Static Random Access Memory**”

Submitted by: **Reem Sherif El Senousy Mohamed**

Degree: **Master of Science in Electrical Engineering**

Abstract

Static random access memory (SRAM) cell design must fulfill a robust operation. In addition, it needs to meet efficient cell area and high speed operation with low leakage while ensuring stability. As a consequence, it is obvious that meeting optimum design constraints for an SRAM cell needs a deeper understanding by the SRAM designers of the engaged trade-offs. In this work, we propose a methodology to model and optimize the 6T SRAM array operation. We model analytically the SRAM array access time for read and write operation at weak inversion.

Meanwhile a new quantitative analysis for the read, write, and hold noise margin of SRAM cells when operated at near-threshold voltages is proposed capturing transistor short-channel effects. Using these derived equations, an optimal design methodology is introduced to yield the SRAM cell size at a certain supply voltage for best noise-margin performance and memory speed. Further, we have proposed a novel figure of merit (FOM) for the device performance used to investigate different parameters impact on SRAM performance. The Overall design is laid out using 65-nm CMOS technology and verified by SPICE simulations.

Acknowledgment

Reem Sherif El Senousy Mohamed

Electronics Engineering and Electrical Communications Department

Faculty of Engineering

Ain Shams University

Cairo, Egypt

07/08/2018

First of all, thanks to ALLAH for everything in my life.

Then, I wish to express my most gratitude to Dr. Sameh Assem Ibrahim for his extensive support. Also I would like to thank Prof. Wagdy Anis and the examiners committee, Prof. Mohamed Amin Dessouky and Prof. El-Sayed Mostafa.

Finally a special thanks goes to my family; my father, my mother and my beloved children; Laila and Malek. I deeply thank my husband Mohamed for his support in every step in my life.

August 2018

Table of Contents

Abstract	xii
1 Introduction	1
1.1 Introduction.....	1
1.2 Problem Statement.....	2
1.3 Thesis Outline.....	3
2 Memory Background	5
2.1 SRAM Architecture.....	5
2.1.1 SRAM Array Structure.....	5
2.1.2 6T- SRAM Cell.....	7
2.1.3 Column Mux and Row Address Decoder.....	7
2.1.4 Pre-charge Circuit.....	9
2.1.5 Sense Amplifier.....	10
2.1.6 Write Driver Circuit.....	10
2.2 6T SRAM Basic Operation.....	12
2.2.1 SRAM bit cell Read Operation.....	12
2.2.2 SRAM bit cell Write Operation.....	13
2.2.3 SRAM bit cell Hold State.....	14
2.2.4 SRAM bit cell design at Strong and Weak Inversion.....	15
2.3 Literature Review.....	16
2.3.1 Strong Inversion Delay/Stability Modeling.....	17
2.3.2 Strong Inversion Delay/Stability Optimization.....	19
2.3.3 Weak Inversion Delay/Stability Modeling.....	20
2.3.4 Weak Inversion Delay/Stability Optimization.....	23
2.3.5 Summary.....	26
3 SRAM Performance Metrics	29
3.1 Stability.....	29
3.1.1 Various Noise Margin Definition.....	33
3.1.2 Read Static Noise Margin (SNM).....	36
3.1.3 Write Noise Margin (WNM).....	36
3.1.4 Hold Noise Margin (HNM).....	37
3.2 Access Time.....	37
3.3 Power and Leakage.....	37