
# CHARGE INDEPENDENT MODELING OF FLOATING GATE MOSFET

By

**Ahmed Hossam Eldin Hamed Hassan**

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of

**MASTER OF SCIENCE**
in
**Electronics and Communications Engineering**

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Under the Supervision of

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**Title of Thesis:**

# Charge Independent Modeling of Floating Gate MOSFET


**Key Words:**

FGMOSFET; Devices Modeling; Parasitic Capacitances; Nano Electronics; Charge Trapping



**Summary:**

This Thesis studies the Floating- Gate MOSFET (FGMOSFET) for its importance in biomedical engineering and many modern low-power applications. A practical DC model for FGMOSFET is highly needed to be used in circuits simulators. A mathematical model for the parasitic capacitances of FGMOSFET in linear and saturation regions of operation is introduced. Then the resultant capacitance values in drain-current equation is applied. In parallel way, a simulation technique in literature for FGMOSFET is stated. Comparison between proposed model and simulation curves are done. The output curves and characteristic curves for FGMOSFET are drawn for various biases. The model proposed is a spice model for FGMOSFET and can be inserted in any circuit simulator such as Spector and various SPICE programs (i.e. HSPICE, WinSPICE, etc.). The model is verified by using 0.13um CMOS technology and Cadence Simulator based on BSIM3 models. The model is based on n-channel FGMOSFET. The model considers velocity saturation as short channel effect and bulk charge due to drain-to-source voltage as second order effect. The model is not a charge conservative. The maximum percentage of error in linear region is 9.6% and in saturation is 2.6%.

# Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Ahmed Hossam Eldin Hamed Hassan Date:

Signature:

## Dedication

To my beloved Parents,

Sisters,

Relatives

and

best Friends.

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# Nomenclature

| | |
|---|---|
| *AC* | Alternative Current |
| *BSIM* | Berkeley Short-Channel IGFET Model |
| *CG* | Control Gate |
| *CMOS* | Complementary Metal-Oxide-Semiconductor |
| *CTF* | Charge-Trap flash |
| *DC* | Direct Current |
| DeFET | Differential electric field sensitive Field Effect Transistor |
| *DIBL* | Drain Induced Barrier Lowering |
| *DSUB* | BSIM Parameter |
| *EEPROM* | Electrically Erasable Programmable Read-Only Memory |
| *eFET* | electric field sensitive Field Effect Transistor |
| EKV | Transistor Model Name |
| ETA0 | BSIM Parameter |
| FAMOS | Field Applied Metal Oxide Semiconductor |
| FB | Flat Band |
| FG | Floating Gate |
| FGMOSFET | Floating Gate Metal Oxide Semiconductor Field Effect Transistor |
| FPGA | Field Programable Gate Array |
| GAA | Gate All Around |
| GB | Gain Bandwidth |

| | |
|---|---|
| MOS | Metal Oxide Semiconductor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NAND | Name of a logic gate |
| QFGMOSFET | Quasi Floating Gate Metal Oxide Semiconductor Field Effect Transistor |
| RAM | Random Access Memory |
| SA | Self-aligned |
| SONOS | silicon–oxide–nitride–oxide–silicon |
| SOS | silicon-on-sapphire |
| SPICE | *Simulation* Program with Integrated *Circuit* Emphasis |
| STI | shallow trench isolator |
| TCAD | Technology Computer Aided Design |