



CHARGE INDEPENDENT MODELING OF FLOATING GATE MOSFET

By

Ahmed Hossam Eldin Hamed Hassan

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE
in
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Title of Thesis:

Charge Independent Modeling of Floating Gate MOSFET

Key Words:

FGMOSFET; Devices Modeling; Parasitic Capacitances; Nano Electronics; Charge Trapping

Summary:

This Thesis studies the Floating- Gate MOSFET (FGMOSFET) for its importance in biomedical engineering and many modern low-power applications. A practical DC model for FGMOSFET is highly needed to be used in circuits simulators. A mathematical model for the parasitic capacitances of FGMOSFET in linear and saturation regions of operation is introduced. Then the resultant capacitance values in drain-current equation is applied. In parallel way, a simulation technique in literature for FGMOSFET is stated. Comparison between proposed model and simulation curves are done. The output curves and characteristic curves for FGMOSFET are drawn for various biases. The model proposed is a spice model for FGMOSFET and can be inserted in any circuit simulator such as Spector and various SPICE programs (i.e. HSPICE, WinSPICE, etc.). The model is verified by using 0.13um CMOS technology and Cadence Simulator based on BSIM3 models. The model is based on n-channel FGMOSFET. The model considers velocity saturation as short channel effect and bulk charge due to drain-to-source voltage as second order effect. The model is not a charge conservative. The maximum percentage of error in linear region is 9.6% and in saturation is 2.6%.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Ahmed Hossam Eldin Hamed Hassan Date:

Signature:

Dedication

To my beloved Parents,

Sisters,

Relatives

and

best Friends.

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Table of Contents

DISCLAIMER	I
DEDICATION	II
ACKNOWLEDGMENT	III
TABLE OF CONTENTS	IV
LIST OF TABLES.....	VI
LIST OF FIGURES.....	VII
NOMENCLATURE	X
ABSTRACT	XII
CHAPTER 1: INTRODUCTION	1
1.1. MOSFET History	1
1.2. Scope of the Thesis	2
1.3. FGMOSFET Applications	4
1.4. Need of modeling	6
1.5. MOSFET Parasitic Capacitances Model	7
1.5.1. Charge independent model.....	7
1.5.2. Charge conservative model.....	12
1.6. Short channel and second order effects	17
1.7. Theory	21
1.7.1. Microstructure of FGMOSFET	21
1.7.2. Basic formulas	23
1.7.3. FGMOSFET Characteristics	25
1.7.4. Various types of FGMOSFET	26
1.8. DC Modeling.....	27
1.9. Problems Concerning FGMOSFET Modeling	30
1.10. Aim of the work	32
CHAPTER 2: MODELING AND SIMULATION.....	33
2.1. Introduction	33
2.2. THE PROPOSED MODELING OF FGMOSFET	33
2.2.1. Charge independent modeling of FGMOSFET	35
2.2.1.1. First approximation: Drain current derivation.....	35
2.2.1.2. Second approximation: floating gate charge derivation.....	37
2.2.1.3. Third approximation: Pinch-off voltage	39
2.3. Simulation Circuit Techniques for FGMOSFET Cell	40
CHAPTER 3: RESULTS AND DISCUSSION.....	43
3.1. Parameters used	43
3.2. Cadence setup	44

3.3. Parasitic Capacitances	45
3.4. DC Characteristic curves	45
3.5. Advantages of proposed model	47
3.6. Disadvantages of the proposed model	47
CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORK	48
REFERENCES	49
APPENDIX A: MATLAB CODES	53
APPENDIX B: CADENCE ENVIRONMENT	62

List of Tables

Table 3.1: Parameters values	42
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List of Figures

Fig 1.1: Conventional MOSFET Structure.....	1
Fig 1.2: FPGA Block Diagram in [1]	2
Fig 1.3: Charge Trapping Device, MNOS Transistor	3
Fig 1.4: Charge Trapping Device, SONOS Transistor.....	4
Fig 1.5: EEPROM Cell.....	4
Fig 1.6: eFET Sensor.....	5
Fig 1.7: DeFET Sensor	5
Fig 1.8: Intrinsic and Extrinsic Capacitances of Conventional MOSFET, as in [20]	7
Fig 1.9: Parasitic Capacitance of MOSFET with $L=5\mu\text{m}$ based on Meyer Model	11
Fig 1.10: Meyer Model for MOSFET illustrated as Equivalent Circuit. g_m and g_{mb} are Gate and Substrate Transconductance. V_{gsi} and V_{bsi} are Gate and Substrate Biases with respect to Source.....	12
Fig 1.11: Charge vs. Gate-to-Source Voltage for BSIM3v3 Model.....	15
Fig 1.12: Capacitances vs. Gate-to-Source Voltage for BSIM3v3 Model	16
Fig 1.13: Charge vs. Drain-to-Source Voltage for BSIM3v3 Model	16
Fig 1.14: Capacitances vs. Drain-to-Source Voltage for BSIM3v3 Model	17
Fig 1.15: Depletion Width at Zero Drain to Source Bias and in Square-Law Model	18
Fig 1.16: Depletion Width with considering Bulk Charge due to Drain to Source Bias as Second Order Effect	18
Fig 1.17: Velocity Saturation as Short Channel Effect vs. Pinch-Off Saturation	19
Fig 1.18: Velocity Saturation meaning including zero Mobility Theory	19
Fig 1.19: Pinch-Off Saturation meaning	20
Fig 1.20: Electron Barrier changes along the Channel.....	20
Fig 1.21: Stacked-Gate Transistor Structure. G is the Control Gate and FG is the Floating Gate	21

Fig 1.22: The Parasitic Capacitances of FGMOSFET and the Control Gate-to-Floating Gate Capacitance, C_{fg}	22
Fig 1.23: The $I_D - V_{DS}$ curves for various values of V_{GS} , solid lines for Model and signs for Experimental Results	25
Fig 1.24: The $I_D - V_{GS}$ curves for various values of V_{DS} , solid lines for Model and signs for Experimental Results. V_{SB} is the Voltage Difference between Source to Body	26
Fig 1.25: Transistor Structure, called FAMOS, that used in some Biomedical Applications.....	26
Fig 1.26: Quasi-FGMOSFET	27
Fig 1.27: NAND Flash Memory used in [27].....	28
Fig 1.28: NAND Flash Memory Cell used in [34]	29
Fig 1.29: Capacitance Coupling Coefficient between Control Gate and Floating Gate vs. both Drain to Source Voltage and Control Gate to Source Voltage in [17]	30
Fig 1.30: Capacitance Coupling Coefficient between Floating Gate and Source vs. Control Gate to Source Voltage in [17].....	30
Fig 1.31: Capacitance Coupling Coefficient between Floating Gate and Body vs. both Drain to Source Voltage and Control Gate to Source Voltage in [17]	31
Fig 2.1: Other Simulation CCT for FGMOSFET Device	39
Fig 2.2: Other Circuit to represent and simulate FGMOSFET Cell.....	40
Fig 2.3: The Simulation CCT used.....	40
Fig 3.1: Cadence Schematic	43
Fig 3.2: Parasitic Capacitances Vs. V_{DS}	44
Fig 3.3: The $I_D - V_{DS}$ curves for $V_{GS} = 1.5, 2, 2.5$ and $3V$, solide line for Model and plus-sign for Simulation	45
Fig 3.4: The $I_D - V_{GS}$ curves for $V_{DS} = 1.5$ and $3V$, line for Model and signs for Simulation.....	45
Fig 3.5: Photo Diode used as the Control Gate of FGMOSFET in [44], (a) Circuit Symbol, (b) Fabrication Diagram.....	46
Fig B.1: Analog Design Environment Simulation for Schematic	61
Fig B.2: Analog Design Environment Simulation View.....	61
Fig B.3: Adding variables from Schematic to Analog Design Environment Simulation by clicking the appropriate button.....	62

Fig B.4: Added variables from Schematic to Analog Design Environment Simulation	62
Fig B.5: Making order to plot Drain Current when Simulation starts.....	63
Fig B.6: Order of Drain Current Plot on Schematic	63
Fig B.7: Order a DC simulation for Drain Current vs. Drain to Source Voltage Sweep	64
Fig B.8: DC Simulation for drain current vs. Drain Current vs. Drain to Source Voltage Sweep ordered in Analog Design Environment Simulation Box	64
Fig B.9: Doing Parametric Analysis from ADE Box	65
Fig B.10: Parametric Analysis Box	65
Fig B.11: Browse the parameter of the FGMOSFET in the Result Browser	66
Fig B.12: Result Browser Box including BSIM3v3 Model Parameters with values according to FGMOSFET Device	66
Fig B.13: Using Calculator to get the Expression for Parasitic Capacitances Waves....	67
Fig B.14: Cadence Calculator Box	67
Fig B.15: Adding Parasitic Capacitances Expressions to ADE to get their values and plot them.....	68
Fig B.16: Parasitic Capacitances Expressions added to ADE.....	68

Nomenclature

<i>AC</i>	Alternative Current
<i>BSIM</i>	Berkeley Short-Channel IGFET Model
<i>CG</i>	Control Gate
<i>CMOS</i>	Complementary Metal-Oxide-Semiconductor
<i>CTF</i>	Charge-Trap flash
<i>DC</i>	Direct Current
DeFET	Differential electric field sensitive Field Effect Transistor
<i>DIBL</i>	Drain Induced Barrier Lowering
<i>DSUB</i>	BSIM Parameter
<i>EEPROM</i>	Electrically Erasable Programmable Read-Only Memory
<i>eFET</i>	electric field sensitive Field Effect Transistor
EKV	Transistor Model Name
ETA0	BSIM Parameter
FAMOS	Field Applied Metal Oxide Semiconductor
FB	Flat Band
FG	Floating Gate
FGMOSFET	Floating Gate Metal Oxide Semiconductor Field Effect Transistor
FPGA	Field Programmable Gate Array
GAA	Gate All Around
GB	Gain Bandwidth

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NAND	Name of a logic gate
QFGMOSFET	Quasi Floating Gate Metal Oxide Semiconductor Field Effect Transistor
RAM	Random Access Memory
SA	Self-aligned
SONOS	silicon–oxide–nitride–oxide–silicon
SOS	silicon-on-sapphire
SPICE	<i>Simulation</i> Program with Integrated <i>Circuit</i> Emphasis
STI	shallow trench isolator
TCAD	Technology Computer Aided Design