HARDWARE IMPLEMENTATION OF A SIMPLIFIED RADIX-4 SUCCESSIVE CANCELLATION DECODER FOR POLAR CODES

By

Hussein Galal Hussein Hassan

A Thesis Submitted to the
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in Partial Fulfillment of the
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Key Words:

Polar codes; Radix-4; partial sum lookahead; simplified successive cancellation decoding; special subcodes;

Summary:

In this thesis, we proposed a latency reduced decoder for the polar codes, this decoder is based on the successive cancellation decoding. The main idea is based on the usage of a radix-4 processing unit to calculate intermediate LLR values, a new last stage processing unit that is capable of decoding more than 4 bits in a cycle and the usage of the partial sum lookahead technique to improve hardware utilization and decrease the overall latency.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute. I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Hussein Galal Hussein Hassan Date:

Signature:

Dedication

I would like to dedicate this thesis for to my parents, my sister, my wife, and my daughters: Malak and Yara for their care, support and extreme patience.

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List of Abbreviations

C	**C**hannel capacity
SC	**S**uccessive **C**ancellation decoder
SCL	**S**uccessive **C**ancellation **L**ist decoder
LR	**L**ikelihood **R**atio
LLR	**L**og **L**ikelihood **R**atio
LTE	**L**ong **T**erm **E**volution
BER	**B**it **E**rror **R**ate
BEC	**B**inary **E**rasure **C**hannel
B-DMC	**B**inary **D**iscrete **M**emoryless **C**hannel
AWGN	**A**dditive **W**hite **G**aussian **N**oise
BP	**B**elief **P**ropagation decoder
Z(W)	Bhattacharyya coefficient
I(W)	Mutual information
W	Transition probability
PU	**P**rocessing **U**nit
LSPU	**L**ast **S**tage **P**rocessing **U**nit

Abstract

Polar codes recently received high attention by researchers as proven to approach channel capacity at higher codeword length. However, the decoding latency grows significantly with codeword length, rendering implementation for latency constrained applications impossible. To tackle this problem, this thesis proposes a polar decoder architecture based on radix-4 processing units with a special last stage processing unit to decode up to 16 bits in the same clock. In addition, it proposes decoding extended special sub-codes to reduce latency. Moreover, it uses partial sum look-ahead technique, resulting in a high throughput with low latency decoding architecture.

Publications

Hassan, Hussein GH, Amr MA Hussien, and Hossam AH Fahmy. "Radix-4 successive cancellation decoding of polar codes with partial sum lookahead." Microelectronics (ICM), 2017 29th International Conference on. IEEE, 2017.

Hassan, Hussein GH, Amr MA Hussien, and Hossam AH Fahmy. "A simplified radix-4 successive cancellation decoder with partial sum lookahead." AEU-International Journal of Electronics and Communications 96 (2018): 267-272.