USING INTERVAL ARITHMETIC FOR ELECTRONIC CIRCUITS SIMULATION

By

Amin Maher Abdallah Baraka

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

USING INTERVAL ARITHMETIC FOR ELECTRONIC CIRCUITS SIMULATION

By

Amin Maher Abdallah Baraka

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Under the Supervision of

Dr. Hossam A. H. Fahmy
Associate Professor
Electronics and Communications Engineering Department
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

USING INTERVAL ARITHMETIC FOR ELECTRONIC CIRCUITS SIMULATION

By

Amin Maher Abdallah Baraka

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

Approved by the
Examining Committee

_____

Associate Prof. Hossam Aly Hassan Fahmy, Thesis Advisor

_____

Prof. Dr. Mohamad Mahmoud Riad El-Ghonemy, Internal Examiner

_____

Prof. Dr. Mohamed Amin Ibrahim Dessouky, External Examiner
Professor at Faculty of Engineering, Ain-Shams University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

Engineer: Amin Maher Abdallah Baraka
Date of Birth: 16/9/1982
Nationality: Egyptian
E-mail: amin.maher@gmail.com
Phone: +20 1011550660
Address: 8 Mohamed AlMahdy St., Nasr City, Cairo

Registration Date: 1/10/2010
Awarding Date: / /
Degree: Master of Science
Department: Electronics and Communications Engineering

Supervisors: Associate Prof. Hossam Aly Hassan Fahmy

Examiners: Prof. Dr. Mohamad Mahmoud Riad El-Ghonemy
Prof. Dr. Mohamed Amin Ibrahim Dessouky
(Professor at Faculty of Engineering, Ain-Shams University)
Associate Prof. Hossam Aly Hassan Fahmy

Title of Thesis: **Using Interval Arithmetic for Electronic Circuits Simulation**

Key Words: interval arithmetic, compact device models, circuit simulation, Monte-Carlo, design variability

Summary:

Semiconductor devices scaling provides higher circuit density and faster devices, this provides better performance and more functionality for electronic chips. Variations affect circuit behavior as more as device scaled down. Verification of circuit behavior under the uncertainty arises from different variations is a challenge. Monte-Carlo statistical analysis and corner case analysis are used to estimate the circuit behavior regards the variations. Interval arithmetic presents a potential alternative to evaluate circuit designs under variations uncertainties.

In this work, we present simulation flow that utilize using of existing designs by replacing statistical parameters variations by interval parameters, so it may replace or enhance the current conventional Monte-Carlo simulation flow. An interval-value based circuit simulation engine is implemented, and library for interval models for sources, linear elements and non-linear elements.

Models library is tested for accuracy against Monte-Carlo simulations. Simulator is tested using linear elements circuits, showing acceptable results for small circuits.

Acknowledgments

First and last I thank god (Allah) for helping me to complete this thesis, and I pray to him to make it a useful work.

I give my appreciation to my mother and father for their encouragement and prayers.

I give a special thanks to my wife who stood to my side and suffered a lot with me through my master study. And a little thanks for my kids

I would like to thank my supervisor Dr. Hossam for his support, guidance and understanding that makes my able to finish this work.

I would like to thank my manger Mohamed Selim for endless help and support and encouragement, and my friends Ahmed Hareedy and Islam Shaboon for their encouragement and advice.

Gratings for my friend Sherif Mansour, the companion through this journey.

My thanks to Mentor Graphics for support and resources.

Dedication

To
My Mother
My Father
and
My Wife

Contents

List of Tables x

List of Figures xi

Symbols and Abbreviations xiii

Abstract xv

1 Introduction 1

1.1 Process Variations 1

1.2 Account For Process Variations 2

1.2.1 Corner Simulations 2

1.2.2 Monte-Carlo Simulation 2

1.3 Research Objective and Contribution 3

1.4 Thesis Organization 3

2 Interval Arithmetic Theories 5

2.1 Classical Interval Arithmetic 5

2.1.1 Historical Notes 5

2.1.2 Notation 5

2.1.3 Definitions and Basic Concepts 6

2.1.4 Order Relations on Intervals 7

2.1.5 Basic Operations of Interval Arithmetic 7

2.1.6 Algebraic Properties of Interval Arithmetic 8
2.1.7 Interval Functions 9
2.1.8 Interval Arithmetic Limitations 9
2.1.9 Interval Arithmetic Tools 10
2.2 Modal Interval Arithmetic 10
2.2.1 Basics 11
2.2.2 Basic Operations of Modal Arithmetic 11
2.2.3 Modal Arithmetic Limitations 12
2.2.4 Modal Arithmetic Tools 12
2.3 Affine Arithmetic 12
2.3.1 Basic Concepts 13
2.3.2 Affine Arithmetic Operations 13
2.3.3 Affine Arithmetic Limitations 16
2.3.4 Affine Arithmetic Tools 16

3 Interval Circuits Simulator Design 17

3.1 Introduction 17
3.2 Simulation flow 17
3.3 Simulator Parts 18
3.3.1 Simulator Front-End 18
3.3.2 Simulator Back-End 21
3.3.3 Simulator Kernel 21
3.4 Simulator Testing 23
3.5 Available Analysis 24

4 Models Library 25

4.1 Voltage and Current Sources 25
4.2 Linear Elements 25

4.3 Non-Linear Elements . . . 28
4.3.1 Techniques to Get Interval Models . . . 28
4.3.2 Simple Diode Model . . . 31
4.3.3 Simple MOSFET Model . . . 34
4.3.4 Advanced MOSFET Models . . . 36

5 Results **37**
5.1 Unit Testing . . . 37
5.1.1 Capacitor Model . . . 37
5.1.2 Diode Model . . . 39
5.1.3 Simple MOSFET Model . . . 40
5.1.4 Advanced MOSFET Models . . . 41
5.2 Passive circuits testing . . . 44
5.2.1 Potential Divider . . . 44
5.2.2 R-2R Resistors Ladder . . . 45
5.2.3 Transmission Line R-C Model . . . 47

6 Conclusion **51**
6.1 Conclusion . . . 51
6.2 Future work . . . 51

Appendix A Interval Algorithms **53**
A.1 Interval Gauss–Seidel Method . . . 53
A.2 Interval Newton Method . . . 54
A.2.1 Multivariate Interval Newton Method . . . 54

Appendix B MVS MOSFET Model Interval Code **57**

References **67**

List of Tables

2.1 Affine Expressions and their interval counterparts 15

3.1 Design with statistical parameters and its interval equivalence 20

3.2 Models library 23

3.3 Simulator tests 23

4.1 Changing $if - else$ conditions to states 29

4.2 Diode model parameters 31

4.3 Verilog-a code for the diode model 31

4.4 C++ code for the diode model interval representation 32

4.5 C++ code for simple MOSFET model interval representation 34

4.6 C++ code for simple MOSFET model affine representation 35

5.1 Diode model parameters values 39

5.2 Diode I_d current model results 39

5.3 MOSFET model parameters values 40

5.4 MVS Test 1 model parameters values 41

5.5 MVS Test 2 model parameters values 42

5.6 MVS Test 3 model parameters values 43

5.7 8-Bits digital to analog converter (R-2R resistors network) simulation results 46

5.8 Transmission line simulation time 47

B.1 C++ code for MVS MOSFET model 57

B.2 C++ definitions for MVS MOSFET model 59

List of Figures

3.1 Monte-Carlo (MC) and interval based circuit simulation flow 19

3.2 Traditional transient simulation flow 22

4.1 Sources functions examples 26

4.2 Voltage source representation with MNA 26

4.3 Resistor representation with MNA 26

4.4 Capacitor model transient equivalent circuit 27

4.5 Another representation for capacitor model equivalent circuit 27

4.6 Inductor transient equivalent circuit 28

4.7 Interval comparing 30

5.1 RC section schematic 37

5.8 Potential divider circuit diagram and equivalent system of equations . . . 44

5.9 Resistor potential divider simulations results 45

5.11 Transmission line R-C model example 47

5.12 Transmission line one R-C section simulations results 48

5.13 Transmission line two R-C section simulations results 48

5.14 Transmission line three R-C section simulations results 49