AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Computer & Systems Engineering

On the Verification of Configurable NoCs in Simulation and Hardware Emulation: A UVM-based Tool

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
Computer & Systems Engineering

by
Sameh Mahmoud Mohamed Aly ElAshry
Bachelor of Science in Electrical Engineering
Communications and Electronics Section
Faculty of Engineering, Alexandria University, 2014

Supervised By
Prof. Dr. Mohamed Watheq Ali Kamel El-Kharashi
Dr. Ahmed Mohammed Mohammed Hamada Shalaby
Dr. Mohamed AbdelSalam Ahmed Hassan

Cairo, 2019

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Computer & Systems Engineering

On the Verification of Configurable NoCs in Simulation and Hardware Emulation: A UVM-based Tool

by

Sameh Mahmoud Mohamed Aly ElAshry
Bachelor of Science in Electrical Engineering
Communications and Electronics Section
Faculty of Engineering, Alexandria University, 2014

Examiners' Committee

Name and affiliation	**Signature**
Prof. Dr. Amr Galaleldin Ahmed Wassal Prof. at Computer Engineering Faculty of Engineering, Cairo University.	.....
Prof. Dr. Ayman Mohamed Mohamed Hassan Wahba Prof. at Computer and Systems Engineering Faculty of Engineering, Ain Shams University.	.....
Prof. Dr. Mohamed Watheq Ali Kamel El-Kharashi Professor at Computer and Systems Engineering Faculty of Engineering, Ain-Shams University.	.....

Date: 17 February 2019

Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain Shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Sameh Mahmoud Mohamed Aly ElAshry
Sameh El-Ashry

.....

Date: 17 February 2019

Researcher Data

Name: Sameh Mahmoud Mohamed Aly ElAshry
Date of Birth: 25/06/1992
Place of Birth: Alexandria, Egypt
Last academic degree: Bachelor of Science
Field of specialization: Electrical Engineering
University issued the degree : Alexandria University
Date of issued degree : 2014
Current job : Digital Verification Engineer, Si-Vision, Cairo, Egypt

Abstract

Network on Chip (NoC) has risen as an interconnection solution for the advanced digital systems, particularly for System on Chip (SoC), because of the huge number of Intellectual Properties (IPs) in the system that need to impart. Different routers and systems have been presented; subsequently the need to make a reusable verification environment to test both single routers and networks. In our thesis, we additionally propose a generic verification environment for NoC using the Universal Verification Methodology (UVM) that tests and verifies both routers and networks in an effortlessly modifiable way to fit different routers and networks.

As opposed to past projections using traditional bus-based interconnections, the utilization of NoC as an interconnection platform has turned out to be more promising to solve complex on-chip communication issues because of what it offers from reusability, scalability and efficiency. Besides, giving a reasonable test base to investigate and verify functionality of any IP core is a necessary stage. To expand; UVM is presented as a reusable and standardized methodology for verifying integrated circuit designs. In our thesis, we begun by introducing an architecture of a complete UVM environment to test generic routers through different test cases giving diverse scenarios to be applied. We likewise intend to establish a base on which other researchers can build to continue towards discovering better solutions.

Error injection has become critically important for testing the reliability of a newly designed hardware system. Evaluating how a Design Under Test (DUT) reacts to different error injection methodologies is very essential for verification engineers to design dependable UVM scoreboards for error-detection purposes. The first main contribution of our thesis is to decide on the feasibility and compatibility of error injection techniques when used with NoC platforms for simulation and hardware emulation environments. We target a UVM-based error injection and detection environment with reusable components. Proposed techniques, introducing both positive and negative test scenarios, are applied to two examples of NoC components: a base router and Daniel router. Base router is a simple case study to prove proposed schemes, whereas Danial router is a complex re-configurable open-source case study. Daniel router provides the ability of changing router architecture with some parameters and applied algorithms. The second main contribution of the thesis is to integrate a full UVM environment with various approaches. Approaches include error injection and detection using reusable and generic UVM environment and components for NoC. Network response is inspected according to error type and methodology.

Finally, the proposed UVM environment is implemented to test and verify an $N \times N$ 2-D or 3-D network composed of base routers or Daniel routers. It calculates the average latency in cycles and the average throughput in packets per cycle per processing element. Both are resolved along a range of injection rates measured in packets per cycle per processing element. The acquired results are compatible with the router efficiency.

Summary

This thesis proposes a configurable verification tool based UVM methodology, scripting and scalable UVM architecture for simulation and hardware emulation environments to test and verify the 2-D or 3-D NoCs with different network sizes, topologies, routing algorithms and flow control methodologies.

The scripted tool supports error injection techniques for NoCs, support automatic detection for the issues through the UVM scoreboards or the functional coverage model, and evaluating NoC architectures.

This thesis presents five contributions. First, we design generic, scalable, and reusable UVM architecture for NoCs using simulation and hardware emulation environments. Second, we apply different error-injection approaches for NoCs through the proposed generic UVM environments. Third, we map of NoC parameters to UVM layers to achieve the re-usability while changing router type. Fourth, we evaluate the base router and Daniel router as different case studies using the generic UVM architecture. Finally, we apply functional coverage technique to catch the source of injected errors.

The thesis is divided into seven chapters, along with list of figures, list of tables, list of abbreviations, and a bibliography.

Chapter 1 introduces the thesis. The background and the motivations of the proposed solution are highlighted. Also, we summarize the contributions of this research.

Chapter 2 summarizes selected research efforts in NoC verification. Most of the research done is about using SystemVerilog as direct testing or using VMM to verify NoC platforms. Nevertheless, we noticed limited research efforts in using advanced verification methodologies in NoC. Also, we did a survey for error injection in some hardware architectures such as memory models, communication modules, and VHDL RTL models. Finally, We show a comparison between the proposed UVM environment and other verification frameworks of open source tools.

Chapter 3 presents the used case studies. We discuss the architecture, specifications and the packet format structure of the used routers such as a base router and a configurable router. Starting with a simple router architecture such as a base router enables proving the ability of building a base structure for the UVM environment to verify NoCs. Then

moving to a complex and configurable daniel router with a different router/network parameters to explain how the change of every parameter affects the proposed UVM environment,the network level parameters are confined between topology, connectivity, and network size. The router level parameters are confined between number of virtual channels per port, packet format, buffer specifications, and packet format. Error injection methodologies are highlighted through both the case studies and the differences are due to architecture and data format variations from the base router to the denial router. We also introduce generic positive and negative verification requirements to verify NoCs.

Chapter 4 explains the proposed generic UVM architectures for NoC platforms for simulation and hardware emulation environments. We present UVM architecture for a single router by describing the UVM components needed to verify a single router, then we introduce UVM environment for NoC simulation purposes by reusing some UVM components from the single router UVM environment to create a UVM environment for NoC. We present UVM environment for NoC hardware emulation for NoC platform by using the same UVM environment created for simulation purposes after adding extra UVM components such as the proxy layer and the transactor interface. We mapping NoC parameters to the UVM layers for reuseability as a novel contribution.

Chapter 5 presents our contribution for NoCs error-injection by explaining the proposed UVM error injection methodologies for NoC platforms for simulation and hardware emulation environments in NoCs such as faulty UVM sequence, faulty UVM reference model, and bus error-injector methodologies. We introduce faulty UVM sequence item or transaction methodology, the approach is a type of a negative testing by sending meaningless data formats to NoC design. We present faulty UVM reference model, this approach is introduced through three types such as faulty Verilog RTL, faulty Verilog netlist, and faulty SystemVerilog model. We introduce bus error-injector agent between routers methodology to corrupt the data inside the network and mimic transmission errors.

Chapter 6 shows our implementation and execution of the UVM environment on a base router and daniel router to measure NoC performance analysis. We present the simulation results and NoC performance analysis results for daniel router and for a base router. We calculate the average latency in cycles and the average throughput in packets per cycle per processing element. Both are resolved along a range of injection rates measured in packets per cycle per processing element. The acquired results are compatible with the router efficiency. We present the response for both routers according to error-injection approaches. We also introduce a functional coverage technique to catch errors.

Chapter 7 summarizes our efforts, document our contributions, and list potential directions for future work for NoC verification.

Keywords: automation, error injection, coverage, functional verification, hardware emulation, measurement, networks-on-chips (NoC), performance, universal verification methodology (UVM).

Acknowledgment

First and foremost, I would like to thank God almighty for giving me the strength, ability, knowledge and chance to embrace this research study and to drive forward and finish it agreeably. Without his blessings, this accomplishment would not have been conceivable.

After a journey towards this degree, I want to express my thanks and gratitude to my advisors, Prof. Dr. Mohamed Watheq Ali Kamel El-Kharashi, Dr. Ahmed Mohammed Mohammed Hamada Shalaby, and Dr. Mohamed AbdelSalam Ahmed Hassan for their support, encouragement and their efforts and guidance to achieve strong contribution and publishing different publications in my thesis.

I want to thank my colleague Mostafa Khamis for his collaboration with me and be responsible for the design side to help me applying my verification ideas on his design.

I wish to thank my wife Shahd Elkabbary for her support towards the defense during the preparation for our wedding.

Finally, I want to thank my family and friends, their supportive words and encouraging messages kept me motivated to work harder and be a better engineer in the academia and the industry.

Sameh Mahmoud Mohamed Aly ElAshry
Computer and Systems Engineering
Faculty of Engineering
Ain Shams University
Cairo, Egypt
February 2019