DESIGN EXPLORATION FOR NETWORK ON CHIP BASED FPGAS: 2D AND 3D TILES TO ROUTER INTERFACE

By

Alaa Salaheldin Gomaa Ibrahim

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
In
Electronics and Communications Engineering

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Under the Supervision of

Prof. Ahmed Mohamed Soliman

Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

Dr. Hassan Mostafa

Assistant Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

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Approved by the Examining Committee

_____
Prof. Ahmed Mohamed Soliman **(Thesis Main Advisor)**
Professor, Faculty of Engineering, Cairo University

_____
Prof. Mohamed Fathy Abu-Elyazeed **(Internal Examiner)**
Professor, Faculty of Engineering, Cairo University

_____
Prof. Ahmed Hassan Kamel Madian **(External Examiner)**
Associate Professor, Nile University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2019

Engineer's Name: **Alaa Salaheldin Gomaa Ibrahim**
Date of Birth: 18/03/1989
Nationality: Egyptian
E-mail: alaa.salaheldin89@gmail.com
Phone: +201065896629
Address: 13rd Abu-Ordia st, Al Basatin,
Cairo, Egypt

Registration Date: 01/10/2012
Awarding Date: / /2019
Degree: **Master of Science**
Department: **Electronics and Communications Engineering**

Supervisors:

Prof. Dr. Ahmed Mohamed Soliman
Dr. Hassan Mostafa

Examiners:

Prof. Ahmed Mohamed Soliman **(Thesis main advisor)**
Professor, Faculty of Engineering, Cairo University

Prof. Mohamed Fathy Abu-Elyazeed (Internal examiner)
Professor, Faculty of Engineering, Cairo University

Prof. Ahmed Hassan Kamel Madian (External examiner)
Associate Professor, Nile University

Title of Thesis:

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Key Words:
Network on Chip, Fields Programmable Gate Array, Router Interface

Summary:

This thesis explores how to adapt and use Networks-on-Chips for designing the next-generation FPGAs, a literature survey of existing Networks-on-Chip designs is presented. A comparative review between three NoC routers is provided it shows that increasing number of router ports affects the area, power and frequency of the network significantly. For that, the Codec is introduced to connect more tiles or modules to the network. A comparison is held between two 2D networks, with and without Codec. Finally, the effects of adding Codec to 3D-NoCs are investigated.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all resources used and have cited them in the references section.

Name: Alaa Salaheldin Gomaa Date: 02/02/19

Signature:

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Alhamdulillah, I praise and thank Allah for giving me the strength and courage to complete this thesis.

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Nomenclature

ASIC	Application Specific Integrated Circuits
BRAM	Block RAM
BSV	Bluespec System Verilog
CLB	Configurable Logic Blocks
DOR	Dimension Ordered Routing
DRAM	Distributed RAM
DSP	Digital Signal Processing
FF	Flip Flop
FPGA	Field Programmable Gate Arrays
IP	Intellectual Property
LUT	Look Up Table
NI	Network Interface
NoC	Network on Chip
NRE	Non Recurring Engineering
PAR	Place and Route
PCF	Physical Constraints File
PDR	Partial Dynamic Reconfiguration
QoS	Quality of Service
RLOC	Relative Location Constraints
SAMQ	Statically Allocated Multi Queue
SoC	Systems on Chip
VC	Virtual Channel

Abstract

Due to the continuous demand for larger and more powerful chips, new blocks are added contentiously to System on Chips (SoCs), such as embedded processors, digital signal processors (DSPs), peripheral interfaces and embedded memory blocks. As the system complexity increases, the negative impact of its routing fabric increases as well. Bus-based and point-to-point interconnects become bottlenecks as they are unable to meet the system requirements. In general, they are not suitable for large systems as their performance degrades when used to connect many blocks. In addition, these interconnects normally include very long wires (global wires) to connect all parts of the chip and these global wires contribute heavily to the increased area and power consumption of the routing fabric.

Field programmable gate arrays (FPGAs) are like SoCs, new blocks and components are continuously added to their architecture in order to meet the increased demand of today's applications. With the increased number of components, the interconnect fabric starts gradually to use Network on Chips (NoCs) to overcome the problems of conventional point-to-point and bus-based interconnects. NoC consists of a network of routers connected with short links, for an FPGA block or tile to connect to another one, it only has to send its data to the nearest router instead of using global wires.

A review for several NoC designs is provided to get an idea about the current research state in this topic. The review is conducted in the context of contributions, architecture, implementation and future work. Then a comparison is held between three NoC routers to analyze the effect of changing the number of Virtual Channels (VCs), flit data width and buffer depth on the consumed area (LUTs and registers) and operating frequency. The comparison shows that the NoC architecture affects the area and maximum operating frequency of the system significantly.

As a result of the mentioned comparison, it is found that one drawback of using NoC is that increasing the router port count affects the area, power and frequency of the system significantly. In order to overcome this problem and to make the NoC approach useful in designing the next generation of FPGAs, a concentrator module or a Codec is proposed to connect between routers and multiple Tiles (FPGA basic building block). Codec reduces the effect of increasing tile count on the area, power and frequency of the routing network.

In order to evaluate the effect of using Codec, a comparison is held between two networks with the same topology and size, one uses routers only and the other uses routers and Codec modules. The comparison is held in the context of area, power and maximum operating frequency. The comparison results show that the area of the Codec network is only 15% compared to the routers only network, its power consumption is 50% less, and operates with 2.5x higher frequency.

Finally, as the three-dimensional integrated circuits technology (3D-IC) is increasingly adopted to cop up with the application demands, the effect of adding Codec to 3D-NoC systems is also investigated.

Chapter 1 : Introduction

1.1. Overview and Motivation

FPGAs (Field Programmable Gate Arrays) are used increasingly in today's applications because of their low development cost, fast design cycle, configurability and short time to market. On the other hand, ASICs (Application Specific Integrated Circuits) have long design cycle, poor configurability and require high development effort. These strong points of the FPGA made it an appropriate candidate for most research and industry applications. However, these advantages come at a significant cost in delay, area and power consumption caused mostly by their programmable routing fabric.

An FPGA mainly consists of three components. Processing elements (PEs), storage elements (SEs) and a complex programmable routing fabric. PEs are programmable logic blocks that perform logic calculations, for example, look-up tables (LUTs) with a fixed configuration of logic gates. SEs are memory blocks placed across the chip area; they are used to store data or algorithm states. The programmable routing fabric is a massive network of wires, multiplexers and bus-based interconnects; all used to connect PEs, SEs and IPs (Intellectual Property cores).

Due to the continuous demand for more powerful and larger chips, new blocks are added to the FPGA architecture, such as Digital Signal Processing (DSP) blocks and embedded processors. As the system complexity increases, the negative impact of the routing fabric increases as well. Bus-based interconnects, such as ARM's AMBA [1] and IBM's CoreConnect [2], become bottlenecks since they are unable to meet the system requirements. In general, they are not suitable for large systems as their performance degrades if used to connect many blocks. In addition, these interconnects include very long wires (global wires) that connect all parts of the chip, these global wires contribute heavily to the increased area and power consumption of the routing fabric.

Network on Chip (NoC) comes as a promising solution for the conventional interconnects problems. NoC has the benefits of independent implementation and optimization of nodes, simplified and customized architecture per application, support for multiple topologies and options, reduced area and power consumption, scalability and increased operating frequency.

Using the NoC approach instead of depending on long interconnect wires solves the conventional interconnect problems because NoC uses high-speed optimized lanes to transfer packets between the routers, and these routers interface with the main application blocks through a configurable number of input/output ports solving most of the problems introduced by long and medium-size routing wires.

Correspondingly, the NoC approach is the right choice as an interconnect fabric for the next generation FPGA. On the other hand, the problems of integrating NoC into the FPGA architecture should be investigated and solved which has been addressed in this research work.