Ain Shams University
Faculty of Engineering
Electronics and Electrical Communications
Engineering Department

Injection-Locked Frequency Multipliers

A Thesis submitted in partial fulfillment for the requirements of
a Master of Science degree in Electrical Engineering
Electronics and Electrical Communications Engineering Department

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B.Sc. of Electrical Engineering
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Statement

This Thesis submitted in partial fulfillment for the requirements of a Master of Science degree in Electrical Engineering, Electronics and Electrical Communications Engineering Department.

The work included in this thesis was carried out by the author at the Electronics and Electrical Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

Mostafa Abdelrahman Hussein Essawy "Injection-Locked Frequency Multipliers", Master of Science dissertation, Ain Shams University, 2019.

The demand for energy-efficient clock generators grows with the spread of internet-of-things (IoT) in our lives. The IoT building blocks are requested to be very efficient so that the battery life could be extended. Besides that, reducing the power consumption of these clock generators in Data Centers leads to a reduction in costs of the electrical and cooling infrastructure of these centers. Moreover, the batteries in the mobile phone platform are considered the main challenge for mobile phone companies. There is a huge trend to reduce the power consumption of frequency multipliers to extend the battery life-time so that we can use a phone for a week and even more without charging it. This thesis aims to design a highly efficient and low power frequency multiplier while suppressing the phase noise using the injection-locked technique. A low-power ring-oscillator-based injection-locked frequency multiplier with a continuous frequency-tracking loop (FTL) that generates 2.4 GHz frequency is proposed. This clock multiplier is designed for wireless local area network (WLAN) applications. A low-power delay cell is used to enhance the

efficiency of the system. The FTL is used for continuous calibration of the ring voltage-controlled oscillator (VCO) frequency drift across process, supply, and temperature variations. The proposed architecture is designed using a 130-nm CMOS process node. Finally, a FoM is reported to compare to all other frequency multiplier designs.

Keywords: Low-power clock multipliers, Injection-locked frequency multiplier, Low-power delay cell, Frequency tracking loop, DCVSL-R cell, phase noise, Phase-locked loops.

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Summary

This thesis is divided into five chapters as follows:

Chapter 1 is an introduction highlighting the frequency synthesizers and emphasizing its importance in many applications such as wireless communication and wireline transceivers.

Chapter 2 includes a survey about different types and architectures of clock generators including conventional PLLs, all-digital PLLs, multiplying delay-locked loops (MDLLs) and injection-locked frequency multipliers (ILFMs), comparing between all architectures in terms of area, power, and noise.

Chapter 3 depicts the different types of injection-locked frequency multipliers and the proposed architecture. System design analysis is demonstrated including the locking range, stability, and noise analyses. This chapter demonstrates all building blocks for the proposed architecture in detail. The chapter ends with the results of superior noise reduction and low power consumption. An FoM is reported in order to compare the proposed solution with other state-of-art architectures.

Chapter 4 introduces the fractional operation challenges and illustrates an efficient solution for this issue. This chapter demonstrates the additional building blocks of the proposed architecture. Also, a technique is adopted to guarantee a calibrator to process, supply, and temperature (PVT) variations. The chapter ends with reporting the results of the proposed architecture and its superior FoM.

Chapter 5 begins with a summary of the thesis and lists its contributions. Finally, the chapter ends by suggesting future work including more optimization and extra features in the proposed Fractional-N ILFM system.

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