



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Department of Computer and Systems Engineering

Obfuscation of Digital Systems using Isomorphic Cells and Split Fabrication

A Thesis submitted in partial fulfillment of the requirements of
the Master of Science Degree in Computer and Systems Engineering
Department of Computer and Systems Engineering

by

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Cairo, 2019



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Statement

This thesis is submitted as a partial fulfillment of the Master of Science degree in Electrical Engineering, Faculty of Engineering, Ain Shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Due to the difficulty for design houses to have their own foundries due to costs and complexity, most design houses tend to outsource the production of their chips to third-party foundries. This could lead to piracy, the insertion of hardware trojans, unauthorized production and usage of chips, as well as other undesired side effects in case the foundries are untrustworthy. It is, therefore, necessary to protect designs against such malicious attempts, while maintaining the design secrets of third-party foundries.

In this study, we reuse the concepts of split fabrication and isomorphic cells to introduce an algorithm for protecting hardware designs against malicious attacks at foundries. Split fabrication aims at splitting designs into two or more different parts that could be designed separately. One of the parts is relatively simple, and could be implemented by a relatively less advanced foundry, which needs to be trusted, and the other part contains the main functionality and usually needs to be implemented by an advanced foundry that is not necessarily trusted.

We combine split fabrication with isomorphic cells, which are generic logic cells that could implement any functionality based on their connections. Split fabrication is applied by disconnecting some vital wires that define the functionality of isomorphic cells, and these connections could be connected later by a trusted foundry.

Experimental results show improvements in security based on several concepts and metrics we introduce in this thesis, and based on other concepts we reuse from recent related work.

Summary

This thesis tackles the problem of hardware security, which has gained increasing attention recently. Due to the difficulty of having their own foundries, most design houses tend to outsource the production of their chips to third-party foundries, which could be untrusted. This could lead to undesired side effects like reverse engineering, piracy, and hardware trojans. Therefore, it is necessary to find ways of protecting IPs (Intellectual Properties) against such malicious attacks.

In this thesis, we contributed to this field by proposing an algorithm for replacing critical gates in designs with generic isomorphic cells that could be configured by a trusted foundry to implement a specific functionality in order to obfuscate designs at advanced foundries which could be untrusted. By combining isomorphic cells and split fabrication, it is more difficult for third parties to achieve any potential malicious goals.

The thesis is split down into six chapters as follows:

Chapter 1 Introduces the problem being studied. Also, we discuss the motivation of this work, and the intended objectives. This chapter also serves as a detailed introduction to the thesis, including a roadmap to the remaining parts.

Chapter 2 summarizes lots of research that has been done into the field of hardware security. The main focus of the mentioned related research is Hardware Trojans, split fabrication, malicious attacks on integrated circuits, protection techniques, and other relevant topics.

Chapter 3 provides a detailed theoretical background. We discuss several concepts reused from recent related work, such as Entropy, Isomorphic Cells, Optimized Isomorphic Cells, and Split Fabrication. We also introduce several new concepts and metrics such as Isomorphic Entropy, Cluster Normalization, Gate Normalization, Cluster Forms, and Truth Table Inclination. All of these concepts serve as a basis for the algorithm we introduce in this work.

Chapter 4 discusses the algorithm at the core of this thesis. The algorithm aims at analysing the effect of each gate on the signal probability of a certain connected cluster of gates. Afterwards, the gates with the highest impact on a design based on several configurable parameters are replaced with isomorphic cells. In this chapter, we discuss our proposed algorithm in detail, including a pseudo code for making things easier.

Chapter 5 provides some information on the designs used as test cases for our algorithm as well as detailed experimental results for each of them. For the scope of this work, we chose several Verilog-based designs as test cases, some of which were implemented by us, and others were reused from other sources. The experimental results include several different metrics for measuring the effect of replacing gates with isomorphic cells based on several configuration parameters. By tuning the configuration parameters, it is possible to get different results, and we provide some examples on this. We also provide some details on the environment setup and the tools used to implement our algorithm.

Chapter 6 summarizes the thesis, including the most important points, and provides hints for potential future work.

Keywords: Hardware Security, Split Fabricaton, Obfuscation, Digital Systems, Foundries, Isomorphic Gates, Reverse Engineering, Piracy.

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