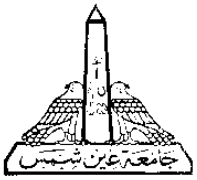

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Electrical Communications Engineering

Injection-Locked Ring Oscillators

A Thesis submitted in partial fulfillment of the requirements of the degree of Master of Science in Electrical Engineering

(Electronics and Electrical Communications Engineering)

by

Eman Salah El-Din Fahmy Ibrahim

Master of Science in Electrical Engineering

(Electronics and Electrical Communications Engineering)

Faculty of Engineering, Ain Shams University, 2019

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Cairo - (2019)

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

This thesis discusses the analysis and the design of an injection-locked ring oscillator for forward-clocking architecture in serial-link transceivers. The injection locking mechanism is analysed and employed in the super-harmonic injection locking scheme.

In this scheme, super-harmonic injection is introduced to a ring oscillator to achieve low phase noise, low rms jitter and a better figure of merit. The ring oscillator was built using Maneatis delay cells for its advantages, like the simple design, high supply/substrate noise rejection and good control over delay.

Simulation results of a 130-nm CMOS design demonstrate the feasibility of the proposed design, achieving the lowest phase noise, jitter and area consumption with respect to many other designs and topologies. It operates at a frequency of 1.52 GHz, with an injection clock of 7.6 GHz. Simulation results show a 58-MHz locking range, achieved with a power consumption of 9.93 mW. Simulation results of RMS jitter, phase noise and phase deskew across a range of oscillation frequencies (1.51 GHz → 1.53 GHz) are illustrated and discussed.

The thesis is divided into five chapters, in addition to lists of contents, figures, tables, abbreviations and symbols, as well as list of references and publications.

Chapter 1

Chapter 1 is an introduction that discusses the evolution of different clocking architectures and an overview of serial-link transceivers, followed by the problem statement and thesis outline.

Chapter 2

Chapter 2 is an introduction to injection locking, its advantages and disadvantages, and the most common design considerations. In addition, a literature survey of different implementations and structures of oscillators and delay cells is included.

Chapter 3

Chapter 3 introduces the proposed architecture and discusses the circuit level of the design in 130-nm CMOS technology.

Chapter 4

Chapter 4 includes the simulation results of the proposed design, in addition to a comparison with other published designs.

Chapter 5

Finally, chapter 5 concludes the thesis and proposes some suggestions for future work.

Key words: Injection Locking, Injection Locked Oscillators, Ring Oscillators, ILO, ILRO, super-harmonic, Maneatis Delay Cell, Phase Noise, Time Jitter.

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Eman Salah El-Din

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