

Ain Shams University
Faculty of Engineering
Electronics and Communications Department

Automatic Analog Layout Router Tool

A Thesis

Submitted in partial fulfillment of the requirements of a Master of Science degree in Electrical Engineering

Submitted by:

Sherif Ahmed Mohamed Abdelfattah

B.Sc. of Electrical Engineering (Electronics and Communications Department)
Ain Shams University, 2012.

Supervised by:

Prof. Dr. Mohamed Amin Dessouky Prof. Dr. Hazem Said Ahmed

Cairo, 2019

Faculty of Engineering – Ain Shams University Electronics and Communications Engineering Department

Thesis Title: "Automatic Analog Layout Router Tool" Submitted by: Sherif Ahmed Mohamed Abdelfattah Degree: Master of Science in Electrical Engineering **Examiners' Committee** Name and affiliation **Signature** Prof. Dr. **El-Sayed Mostafa Saad** Electronics and Communications Dept. Faculty of Engineering, Helwan University Prof. Dr. Hani Fikry Ragai Electronics and Communications Dept. Faculty of engineering, Ain Shams University Prof. Dr. **Mohamed Amin Dessouky**

Electronics and Communications Dept.

Faculty of Engineering, Ain Shams University

Date: 2/11/2019

Statement

This dissertation is submitted to Ain Shams University for the degree of

Master of Science in Electrical Engineering (Electronics and

Communications Engineering).

The work included in this thesis was carried out by the author at the

Electronics and Communications Engineering Department, Faculty of

Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any

other university or institution.

Name: Sherif Ahmed Mohamed Abdelfattah

Date: 2 / 11 / 2019

Curriculum Vitae

Name: Sherif Ahmed Mohamed Abdelfattah

Date of Birth: 25/11/1989

Place of Birth: Cairo, Egypt

First University Degree: B.Sc. in Electrical Engineering

Name of University: Ain Shams University

Date of Degree: June 2012

ACKNOWLEDGEMENT

Thanks Dr. Dessouky for your great efforts in guiding me through my thesis work, starting from making the survey, and choosing the programming language and working on the layout automation scripts till the end with publishing our papers and writing the documentation.

I would like to thank my research group colleagues who worked closely with me and gave me some hints during scripting and publishing the papers, Especially Fady Atef, Inas Mohamed, and Soha Hamed.

Also, I want to say thanks for my work colleagues who supported me by sharing their knowledge in research and master's process, especially Bahaa Ragheb, Amr Abdelhadi, Mostafa Fouad and Ahmed Gamal.

I can't forget the great favor my parents have done to me, by supporting me during all my life events starting from school till the master's degree.

Sherif Ahmed

Cairo, Egypt

2-November-2019

ABSTRACT

This thesis presents a new analog layout automation tool. Devices are placed according to satisfiability modulo theories, which checks the feasibility of the layout constraints equations. Placer generates multiple solutions to let the user choose the best one. Then the routing channel estimator checks the needed routing channels dimensions and the area increase due to these routing channels for these multiple placer outputs. Then the user can choose the best solution after the routing channel estimator. This step will be more accurate from choosing the best solution after the placement and it will be faster from choosing after the router. After the routing channel estimator calculates the needed routing channels dimensions the routing channel locator increases the spacing between devices according to the routing channels` sizes then the router works on the main cells like current mirrors and differential pairs. Then it works on top level routing, with taking into consideration the matching between routes, DRC, LVS rules, and the electro-migration specifications.

SUMMARY

Faculty of Engineering – Ain Shams University

Electronics and Communications Engineering Department

Thesis Title: "Automatic Analog Layout Router Tool"

Submitted by: Sherif Ahmed Mohamed Abdelfattah

Degree: Master of Science in Electrical Engineering

The need for analog layout automation is increasing significantly through the previous couple of decades due to the increasing design specifications and the new technologies. A lot of automation tools for the digital layout exist now in the market but they are not completely reliable, and the analog layout automation isn't complete yet. That is due to the higher complexity in the analog layout starting from the different devices' sizes and their lot of tradeoffs and requirements to meet the design specifications.

In this thesis, placement is done using Satisfiability Modulo Theories "SMT". These theories check if some equations have feasible solutions and return the values of these equations variables where they satisfy these equations. These SMT equations are checked using Z3 SMT solver and generate a different number of solutions.

The router checks the needed area increase due to the routing channels between devices, such that the user can choose the best solution according to the area and the aspect ratio. Then the router increases the spacing between devices of the selected placer outputs and then adds the needed routes, vias, and guard rings.

This thesis is divided into six chapters as follows:

Chapter 1:

This chapter presents a brief introduction to this thesis and the need for layout automation. It also shows the automation effort done and its main algorithms which is divided into placer using satisfiable modulo theories and then the routing.

Chapter 2:

The automation process survey is presented in this chapter. It started with the main automation algorithms and the floor planning techniques. Then it illustrates the popular routing algorithms and the way of presenting the layout data through the automation process for faster processing.

Chapter 3:

In this chapter a survey of some of the available automation tools are presented. Then it presents the SMT algorithm and its difference from ordinary SAT theories. Then how the layout constraints are converted into mathematical equations suitable for the SMT theories. Then it presents the exact placement flow used in the tool scripts.

Chapter 4:

In this chapter, the proposed auto-routing effort is discussed. The auto-router starts by estimating the spacing needed between devices suitable for the routing channels for devices routes and top-level routes. Then it increases spacing accordingly using the routing channel locator. After increasing the spacing, the router starts by adding the needed routes, via devices, and guard rings.

Chapter 5:

This chapter presents different experimental results of the auto-placement and routing tool in this thesis.

Chapter 6:

Conclusion and suggested future work for this layout automation tool is presented in this chapter.

CONTENTS

ACKI	WON	LEDGEM	IENT	I
ABS	ΓRAC	т		III
SUM	IMAF	RY		.V
CON	TENT	S	\	/II
LIST	OF F	IGURES		ΧI
LIST	OF T	ABLES	Χ	(V
ABBI	REVI	ATIONS	X\	/II
1 IN	ITRO	DUCTIO	N	. 1
	1.1	LAYOUT A	Automation	. 1
	1.2	SMT PLA	ACER	. 1
	1.3	ROUTER.		. 2
	1.4	THESIS OF	RGANIZATION	. 2
2 B	ACKO	ROUND		. 7
	2.1	Introdu	CTION	. 7
	2.2	FLOORPLA	AN REPRESENTATIONS	. 8
		2.2.1	Absolute representation	8
		2.2.2	Topological representations	8
	2.3	Аитома	TIC LAYOUT GENERATION	LO
		2.3.1	Procedural algorithms	. 10
		2.3.2	Template algorithms	.10

	2.3.3	3 Optimization algorithms	12
	2.4 AUTON	MATIC ROUTING	13
	2.4.2	1 Routing algorithms	13
	2.4.2	2 Routing representations	17
	2.5 Ѕимм	IARY	23
3	LITERATURE	REVIEW	27
	3.1 Introd	DUCTION	27
	3.2 AVAILA	ABLE TOOLS	27
	3.2.2	1 LAYGEN II	27
	3.2.2	2 KOAN/ANAGRAM II	29
	3.2.3	3 ALSYN	30
	3.2.4	4 ILAC	31
	3.2.5	5 ALADIN	32
	3.2.6	6 ALG	33
	3.2.7	7 IPRAIL	34
	3.2.8	8 LAYLA	35
	3.2.9	9 Zhang	35
	3.3 SMT P	PLACER	37
	3.3.2	1 SAT	37
	3.3.2	2 SMT	39
	3.3.3	3 Mapping constraints into equations	39
	3.3.4	4 Proposed placement flow:	48
	3.4 SUMM	IARY	51
4	PROPOSED A	AUTO-ROUTING FLOW	55
	A 1 INTRO	DUCTION	55

	4.2	PROPOSED	LAYOUT SYSTEM FLOW	. 56
	4.3	Intra-Dev	VICE ROUTING	. 56
		4.3.1	Channel estimator	56
		4.3.2	Channel locator	60
		4.3.3	Device router	61
	4.4	INTER-DE	/ice Routing	. 66
		4.4.1	Channel estimator	66
		4.4.2	Channel locator	68
		4.4.3	Top-level router	68
	4.5	Summary	· · · · · · · · · · · · · · · · · · ·	.72
5	RESUL	TS		.74
	5.1	Introduc	TION	.74
	5.2	SINGLE-EN	DED SINGLE-STAGE OTA	. 74
		5.2.1	Inputs and constraints	74
		5.2.2	Placer outputs	75
		5.2.3	Router outputs	76
		5.2.4	Other possible user constraints output	78
	5.3	FOLDED CA	ASCODE OTA	. 80
		5.3.1	Inputs and constraints	80
		5.3.2	Placer outputs	81
		5.3.3	Router outputs	82
		5.3.4	Other possible user constraints outputs	86
6	SUMN	1ARY AND	FUTURE WORK	.90
	6.1	Summary	′	. 90
	6.2	Suggeste	D FUTURE WORK	.95

APPENDIX99				
INPUT FILES	99			
RUN FILES	99			
PLACER SCRIPTS	101			
ROUTING CHANNEL ESTIMATOR AND LOCATOR SCRIPTS	101			
DEVICE ROUTER SCRIPTS	101			
TOP LEVEL ROUTER SCRIPT	102			
BIBLIOGRAPHY	104			