AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Charge-Steering Circuits for Low-Power Applications

A Thesis submitted in partial fulfilment for the requirements of a

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Khaled Mohamed Abdel Hafez Abdel Aal Hassan

Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2019
Supervised By

Prof. Emad Eldin Mahmoud Hegazi

Assoc. Prof. Sameh Assem Ibrahim

Cairo - (2019)

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications

Charge-Steering Circuits for Low-Power Applications

by

Khaled Mohamed Abdel Hafez Abdel Aal Hassan

Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2013

Examiners' Committee

Name and Affiliation	**Signature**
Prof. Mohamed Ibrahim Aladawy Salama Faculty of Engineering, Cairo University, Electronics and Communication Engineering Dept.	……..
Prof. Mohamed Amin Dessouky Faculty of Engineering, Ain Shams University, Electronics and Communication Engineering Dept.	……..
Prof. Emad Eldin Mahmoud Hegazi Faculty of Engineering, Ain Shams University, Electronics and Communication Engineering Dept.	……..
Assoc. Prof. Sameh Assem Ibrahim Faculty of Engineering, Ain Shams University, Electronics and Communication Engineering Dept.	……..

Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering and Communications Engineering Department, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Student name: Khaled Mohamed Hassan

Signature

……

Acknowledgement

All praise is due to Allah, Most Merciful, the Lord of the Worlds. I would like to thank God Almighty for bestowing upon me the chance, strength and ability to complete this work.

I would like to express my gratitude to all my family who always supports and encourages me in my career path. Many thanks to my supervisors Prof. Emad Hegazi and Prof. Sameh Ibrahim for their guidance, wise advice, useful suggestions, continuous motivation, and feedback.

I am very grateful to all the IC Lab professors and my first career mentor, Mohamed Tawfik, Principle Engineer Si-Vision. I'd like also to thank Eng Ahmed Saad, Eng Ahmed Salah, Eng Mohamed Samir and Eng Mohammed Tawfik for giving me the opportunity to work as an Analog/RF Design engineer at Si-Vision. This industrial experience and lab testing across different nodes directly improve my knowledge and skills in the IC Design. Finally, I can’t forget the favour of my dear colleagues Macro Adel, Mostafa Toubar, Omaira Hamada, Hazem Hassan, Bishoy Malid, Mostafa Hosny, Ahmed Mansour, Andrew Mikheal, Mohamed Fouad, Mahmoud Abdel Wahab, Mostafa Salem, Mostafa Fouad, Ahmed Gharib, Ahmed El-Sayed, Ahmed Rafeet, Omar Hamada, Amr Ahmed and Ahmad Yassin for the many technical discussions and their continuous support.

Khaled Mohamed Abdel Hafez Abdel Aal Hassan

Electronics and Communications Engineering Department Ain Shams University, Cairo, Egypt

September 2019

Researcher Data

Name	: Khaled Mohamed Hassan
Date of birth	: 03/10/1991
Place of birth	: Cairo, Egypt
Last academic degree	: B.Sc. in Electrical Engineering
Field of specialization	: Electronics and Communications
University issued the degree	: Ain Shams University
Date of issued degree	: September 2013
Current job	: Member of Technical Staff at Vidatronic.

Summary

This thesis aims to study and design charge-steering (CS) circuits for different applications. The thesis is divided into two main parts design of CS circuits for high-speed wireline transceivers and the study of energy-delay curves for different types of flip-flops (FFs). The thesis consists of five chapters including lists of contents, tables and figures as well as list of references.

Chapter 1

Chapter 1 gives a brief introduction to the motivation, objectives, major contributions and organization of the thesis.

Chapter 2

Chapter 2 presents a literature survey for wireline transceivers and discuss the prior art for low-swing FFs. The analysis and design of low-swing FF are discussed thoroughly in this chapter.

Chapter 3

Chapter 3 shows the proposed CS circuits to enhance the power efficiency of the high-speed wireline receiver. Two newly proposed CS FFs along with a CS based DFE are presented and discussed thoroughly.

Chapter 4

The analysis and comparison of different FFs types are discussed in this chapter. The design variables are separated for each FF into dependent and independent design variables. The optimization using energy-delay curves using a unified methodology is introduced for both low-swing FFs and rail-to-rail FFs.

Chapter 5:

The conclusions for this work are given. Suggested future work including optimization or extra features are also shown.

Keywords: Charge-Steering, Flip-Flop, High Speed Serial Links, Wireline Transceivers, Current-Mode-Logic.

Abstract

This thesis aims to study the design of charge-steering (CS) circuits for different applications. The thesis is divided into two main parts; design of CS circuits for high-speed wireline transceivers and the study of energy-delay curves for different types of flip-flops (FFs).

CS circuits are known for their superior performance over current-mode-logic (CML) counterparts. However, different CS circuits suffer from several disadvantages. CS circuits suffer from at least one of the three following disadvantages; inter-symbol interference (ISI), output not being valid for the entire cycle requiring a special clocking system, or no enough gain. Thus, the usage of CS circuits is somehow limited due to cascading issues. In this thesis two newly CS FFs are introduced, the proposed CS FFs overcome the above-mentioned disadvantages. Implemented in a 65-nm CMOS technology, the 1st proposed CS FF consumes 660 μW at a data rate of 30 Gb/s from a 1-V supply, meanwhile the 2nd proposed CS FF consumes 520 μW at a data rate of 25 Gb/s from a 1-V supply. Meanwhile the 2nd proposed CS FF is utilized in a CS DFE, the total power consumption of the CS DFE is 0.68 mW resulting in a power efficiency of 0.034 pJ/bit which is better than any other DFE published before.

The thesis includes a comparison between different types of FFs. FFs can be divided into two types; low-swing FFs and rail-to-rail FFs. The comparison is done through using energy-delay curves. Finding the optimum sizing for an FF using energy-delay curves was limited before to rail-to-rail FFs only. Low-swing FFs were optimized as a purely analog/Radio-Frequency (RF) circuits. The thesis proposes to extend the analysis and the comparison to low-swing FFs as well. Low-swing FFs can be divided into two main branches; CML and CS. A unified methodology is used to define the dependent and independent design variables for each FF, afterwards an optimization is carried over to define the optimum sizing for different energy and delay weighting.

Table of Contents