



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Blocker Tolerant Sigma Delta ADC

A Thesis submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

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Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2014

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Cairo - (2019)



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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

This thesis illustrates an overview of blocker tolerant analog to digital converters and shows the need of this type of modulator in the communication system and its benefit of reducing the analog receiver complexity. The new technique enables the sigma-delta analog to digital converters (SDADC) to withstand blockers at certain frequency, without saturation. The technique relies on adding a notch filter within the SDADC that affects the signal transfer function (*STF*) without affecting the noise transfer function (*NTF*).

Different topologies of the blocker tolerant modulator are illustrated. A new approach is studied in the discrete time which is characterized by its filtering property of the blocker at specific frequency, then implemented in the continuous time.

For a WiMax system, the sampling frequency is chosen to be 256MHz, signal Bandwidth 2MHz. The system idea is performed using linear models on MATLAB, to study the effect of the proposed idea on the modulator. Two approaches have been tested in the discrete time and one is chosen to be implemented in the continuous time. The system is then transferred to transistor level using 65nm CMOS technology.

Simulation results show that the proposed technique enables the SDADC to withstand a large blocker level without degrading the peak signal to noise ratio (*SNR*) and improving the *SNR* by at least 10 dB when compared to the case with no blocker rejection. The modulator operates at supply 1.2V and 2.5V for the feedback DAC.

The thesis is divided into five chapters including lists of contents, tables and figures as well as list of references.

Chapter 1

In this chapter an introduction about the need of blocker tolerant modulators has been viewed, including a quick overview on the main idea and main contributions of this work.

Chapter 2

This chapter consists of two parts. In the first part a brief overview of sigma delta modulators ($\Sigma\Delta M$) is presented. The second part is the main reasons of interest in continuous time (CT) modulators. Finally, in this chapter, a quick overview on blocker tolerant ADC and the state of the art of continuous time blocker tolerant $\Sigma\Delta ADC$ is viewed.

Chapter 3

This chapter consists of three parts. The first part introduces the proposed idea of sigma delta modulators ($\Sigma\Delta M$) and testing it in the discrete time and then transfer to the continuous time. The second part is illustrating the system under the effect of the DAC

delay that arises from the circuit design. The last part discusses the modeling of the integrator Non-ideality.

Chapter 4

This chapter shows the design methodology of the system using technology 65nm CMOS, where it is divided into two parts. The first part illustrates the implementation of three main subparts which are the 1-bit quantizer, the DAC (DT part) and the system integrators (CT part). In the second part the system is tested after the blocks integration and results are viewed.

Chapter 5

It presents a summary for the dissertation, along with possible directions for future work.

Keywords: Blocker tolerant continuous time sigma delta ADC.

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LIST OF SYMBOLS

C_i	Unit capacitance value	F
C_f	S.C feedback capacitance	F
C_{ox}	MOS transistor oxide capacitance	F
Δ	LSB step size	V
$e[n]$	Sigma delta effective quantization error	V
f_{in}	Input frequency	HZ
f_{in}	Sampling frequency	HZ
g_m	Transistor intrinsic trans-conductance	A/V
I_D	MOS transistor drain current	A
μ_n	NMOS transistor electron mobility	$m^2/V \text{ sec}$
τ	Time – constant	sec
V_{cm}	Common mode voltage	V
V_{DD}	Supply voltage	V
V_{GS}	Gate-source voltage	V
V_e	Quantization error voltage	V
w_o	Notch frequency	rad/sec
α	Scaling factor	---
V_{in}	Input voltage	V
V_{thn}	Threshold voltage of an NMOS transistor	V
V_{thp}	Threshold voltage of an PMOS transistor	V
$X(Z)$	Z-transform of $x(t)$	---
$X(S)$	La Place-transform of $x(t)$	---

ABBREVIATIONS

ADC	Analog to Digital Converter
BW	Band Width
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DAC	Digital to Analog Converter
DR	Dynamic Range
DT	Discrete Time
ENOB	Effective Number Of Bits
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
FoM	Figure of Merit
LSB	Least Significant Bit
NTF	Noise Transfer Function
PSD	Power Spectral Density
SDADC	Sigma Delta Analog to Digital Converter
SNR	Signal to Noise Ratio
SNDR	Signal to Noise plus Distortion Ratio
STF	Signal Transfer Function
VFS	Full scale voltage