



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

بسم الله الرحمن الرحيم



MONA MAGHRABY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم



شبكة المعلومات الجامعية التوثيق الإلكتروني والميكروفيلم



MONA MAGHRABY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

جامعة عين شمس التوثيق الإلكتروني والميكروفيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأقراص المدمجة قد أعدت دون أية تغييرات



يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار



MONA MAGHRABY



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Gigahertz Data Converters

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by

Sherif Ahmad Mohammad Ghozzy
Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2016

Supervised By

Prof. Dr. Hani Fikry Ragai
Dr. Mohamed Ahmed Mohamed El-Nozahi

Cairo, 2020



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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Sherif Ahmad Mohammad Ghozzy

Signature

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Date:/...../.....

Researcher Data

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Last academic degree: Bachelor of Science

Field of specialization: Electronics Engineering and Electrical Communications

University issued the degree : Ain Shams University

Date of issued degree : June 2016

Current job : Teaching assistant at Faculty of Engineering, Ain Shams University

Thesis Summary

The thesis is divided into five chapters besides the list of contents, figures, tables and list of references.

Chapter 1:

In this chapter, an introduction that discusses the drives and motives behind Gigahertz Data Converters is presented. Interesting properties of time-based analog to digital converters are then discussed. Next, the objectives of this thesis and its contributions are demonstrated.

Chapter 2:

In this chapter, a brief qualitative and quantitative analysis of VCO-based ADCs is presented. Several VCO-based ADC architectures that address the VCO non-linearity issue are then discussed, highlighting their respective advantages and disadvantages.

Chapter 3:

Chapter 3 proposes a new architecture that addresses the VCO non-linearity issue in an open-loop fashion. It utilizes the conventional two-step residue cancelling technique presented in prior art. Qualitative and quantitative analysis of the proposed system and the associated non-idealities are presented to verify the validity of the proposed architecture, supported by behavioral simulation results.

Chapter 4:

Chapter 4 discusses circuit design of the proposed architecture. It explores implementation of each building block, along with simulation results for each block and for the complete architecture.

Chapter 5:

Chapter 5 summarizes the thesis and focuses on its contributions and outcomes. It concludes the thesis with suggested future work.

Key words:

Analog-to-digital converter, delta-sigma ADC, distortion cancellation, high bandwidth, highly digital, active filters, low-power, nonlinearity mitigation, open loop, power efficient, Pulse width modulation, time-domain ADC, two-step VCO based ADC, VCO based quantizer, voltage swing reduction

Abstract

**Faculty of Engineering – Ain Shams University
Electronics and Communication Engineering Department**

Thesis title: **”Gigahertz Data Converters”**

Submitted by: **Sherif Ahmad Mohammad Ghozzy**

Degree: **Master of Science in Electrical Engineering**

Abstract

With Complementary Metal Oxide Semiconductor (CMOS) technology scaling, the feature size of the transistor becomes smaller which enhances the speed of the transistors. The shrinkage of the device dimensions also reduces the dynamic power consumption of the digital circuits, which is often the dominant power consumption in CMOS logic. However, analog circuit design is harmed by these changes. The supply voltage needs to be reduced to preserve the bearable electric field across the scaled transistor channel, which creates weak overdrive voltages across the gate-source potential of the transistors, making them slower. Moreover, the transistors need to be sized far from the minimum dimensions to guarantee a low noise floor that would not override the received signal, which would call for larger current values to be capable of efficiently driving the parasitic capacitances associated to these transistors. Thus, the design of highly accurate voltage-based analog circuits becomes increasingly challenging with technology advancement and in particular the design of voltage-based ADCs.

On the other hand, time-based ADCs benefit from the down scaling of the transistor dimensions as the time resolution is enhanced. Due to their highly digital nature, the speed of such ADCs can easily reach up to giga samples per second speed while typically consuming less power than the voltage-based equivalents. One such class of time-based ADCs is the Voltage Controlled Oscillator (VCO)