



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

بسم الله الرحمن الرحيم



MONA MAGHRABY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم



شبكة المعلومات الجامعية التوثيق الإلكتروني والميكروفيلم



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جامعة عين شمس التوثيق الإلكتروني والميكروفيلم

قسم

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AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Generalized Approach for Automatic Analog Layout

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Soha Sherif Samir Hamed

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Ain Shams University, 2012

Supervised By

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Cairo - (2020)



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Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering , Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Analog layout has always been a complicated, time consuming process. This is due to the numerous barriers faced in layout including routing or interconnect parasitics, mismatch effects for critical devices, routes...etc. If any of these issues is ignored, chips after fabrication may not provide the required specifications needed by the designer. Hence, affecting the overall yield and competitive advantage in the IC industry. Furthermore, as technology nodes go further into deep sub-micron nodes, the effect of such mismatches amplifies exponentially.

Therefore, this thesis proposes a flow to place and route some of the most important device groups; current mirrors and differentials pairs. The proposed flow takes into consideration the issues mentioned earlier; parasitics and mismatch sources. It is a time saving, reliable, user-controlled flow for analog layout automation tools. The routing flow comes an as a complementary part to an algorithm responsible for devices placement using an adapted form of genetic optimisation.

The thesis also proposes a procedural router to route a complete circuit's sub-blocks such as OTAs.

Key words:

Layout, Automation, Matching, Current mirror, Systematic, Random, Mismatch, STI, Optimization, Genetic algorithm, Place-ment, Modeling, Segmented Integral model, Constraints, Cell-level.

Summary

The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references.

Chapter 1

This chapter is an introduction explaining the need for layout automation tools and the outline of this thesis.

Chapter 2

This chapter includes a survey of the latest layout automation tools, mismatch sources affecting layout design, current mirror systematic mismatch modelling, and finally the STI evaluation flow. The chapter also includes an explanation of the genetic algorithm concept and phases.

It also explains the placer which is used to generate an optimal pattern for the current mirror. It explains in detail how the patterns are generated using segmented integral model and the genetic optimization used in current mirror mismatch calculation.

Chapter 3

In this chapter matched analog device router tool is explained. It also explains how the routes are generated and the constraints are considered to ensure the best matching environment.

Chapter 4

This chapter explains the procedural router needed to route an OTA of any architecture.

Chapter 5

This chapter shows practical examples where the tool has been applied and the results produced.

Chapter 6

This chapter ends the thesis by conclusions, summary and future work.

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