بسم الله الرحمن الرحيم

MONA MAGHRABY

شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

شبكة المعلومات الجامعية

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جامعة عين شمس

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قسم

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MONA MAGHRABY

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Analog Layout Router for Sub-nm Manufacturability

A Thesis

submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Fady Atef Naguib Nasr

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2007

Supervised By

Prof. Dr. Mohamed Amin Dessouky

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Date: 29th of February 2020

Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Analog circuits are essential part of nearly all the IC industry making nearly 15% of the share of its market. The process of analog IC design is known to be time consuming and error prone. According to a statistical data published by Electronic Design Automation EDA weekly on 2005, Analog design takes nearly 40% of the design effort and causes about 50% of the errors found. This is although analog components represent usually only 3% of the area in system-on-chip designs.

This thesis presents a new analog layout design tool for placement and routing of circuits, the main scope is to build a complete routing tool but from the research we have proved that placement and routing are totally dependent on each other. For placement tool we developed innovative template algorithm to decrease the solution space in an effective way then an optimization method to choose the best placement using satisfiability modulo theories SMT linear Solver, then the tool start the routing phase in two steps the first to route the main sub-blocks as will be identified through the thesis and the second step by using an enhancement Dijkstra algorithm to find the shortest path and taking into consideration more layout constraints like parasitic, electromigration, Manhattan routing techniques, ..etc.

This tool built in a way to consider the most advanced techniques used in today`s industrial products as well today advanced deep nodes to decrease the design cycle and layout iterations. This tool extracts the main sub-blocks types from the schematics then starts processing on each sub-block like current mirrors and differential pairs, to find the best matching pattern that satisfies the block constraints and estimate the needed routing taking the parasitic into consideration, then checking the available space for routing between blocks using a modified Dijkstra Algorithm to find the shortest path between the connected pins, and finally the tool draw the actual routes and placed them in the layout view.

Thesis Summary

The EDA solutions made to facilitate the work of analog designers are very limited and outdated. This was due to the focus given through the last decades for digital circuits in accordance with Moore's law. Also, the fact that analog design is very sensitive to various effects and involves multiple designing constraints that are not found in its digital counterpart. Analog design is of a heuristic nature and knowledge intensive. Luckily, with more reports on how analog design has become the bottle neck of IC design, now, EDA companies are shifting their focus and intensifying their efforts to automate Analog circuit design.

Analog design consists primarily two paths, top-bottom electrical path and bottom-up physical path. The physical path consists of layout generation and verification. Layout generation has reported to cause nearly 30% deviation of the electrical results in small nodes (20 nm and below). Hence, it is of very critical importance to seek automation solutions for the layout generation problem.

The thesis is divided into five chapters in addition to the lists of contents, tables and figures as well as list of references and one appendix.:

- Chapter 1: Introduction to Analog Circuit Layout Generation
    - Presents a brief introduction to the area of analog IC design automation, with special emphasis to the automatic layout generation.
- Chapter 2: Literature Review on the-State-of-the-Art Solutions
    - Present the placement and routing problem in the EDA and a brief overview of the most recent tools developed in this field.
- Chapter 3: Proposed Automation Flow
    - Gives an overview of the proposed automatic flow for analog IC design, with emphasis on the layout generation task
- Chapter 4: Results & Discussions
    - The flow will be demonstrated on a differential operational transconductance amplifier "OTA"
- Chapter 5: Conclusion & Future Work

Key words: Analog Layout, Automation, Analog Constraints, Integrated Circuits, Placement, Matching, Satisfiability Modulo Theories, Analog Routing.

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