



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكرو فيلم

بسم الله الرحمن الرحيم



MONA MAGHRABY



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جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

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MONA MAGHRABY



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Analog Layout Router for Sub-nm Manufacturability

A Thesis

submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Fady Atef Naguib Nasr

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2007

Supervised By

Prof. Dr. Mohamed Amin Dessouky

Dr. Hazem Said Ahmed

Cairo - (2020)



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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Analog circuits are essential part of nearly all the IC industry making nearly 15% of the share of its market. The process of analog IC design is known to be time consuming and error prone. According to a statistical data published by Electronic Design Automation EDA weekly on 2005, Analog design takes nearly 40% of the design effort and causes about 50% of the errors found. This is although analog components represent usually only 3% of the area in system-on-chip designs.

This thesis presents a new analog layout design tool for placement and routing of circuits, the main scope is to build a complete routing tool but from the research we have proved that placement and routing are totally dependent on each other. For placement tool we developed innovative template algorithm to decrease the solution space in an effective way then an optimization method to choose the best placement using satisfiability modulo theories SMT linear Solver, then the tool start the routing phase in two steps the first to route the main sub-blocks as will be identified through the thesis and the second step by using an enhancement Dijkstra algorithm to find the shortest path and taking into consideration more layout constraints like parasitic, electromigration, Manhattan routing techniques, ..etc.

This tool built in a way to consider the most advanced techniques used in today`s industrial products as well today advanced deep nodes to decrease the design cycle and layout iterations. This tool extracts the main sub-blocks types from the schematics then starts processing on each sub-block like current mirrors and differential pairs, to find the best matching pattern that satisfies the block constraints and estimate the needed routing taking the parasitic into consideration, then checking the available space for routing between blocks using a modified Dijkstra Algorithm to find the shortest path between the connected pins, and finally the tool draw the actual routes and placed them in the layout view.

Thesis Summary

The EDA solutions made to facilitate the work of analog designers are very limited and outdated. This was due to the focus given through the last decades for digital circuits in accordance with Moore's law. Also, the fact that analog design is very sensitive to various effects and involves multiple designing constraints that are not found in its digital counterpart. Analog design is of a heuristic nature and knowledge intensive. Luckily, with more reports on how analog design has become the bottle neck of IC design, now, EDA companies are shifting their focus and intensifying their efforts to automate Analog circuit design.

Analog design consists primarily two paths, top-bottom electrical path and bottom-up physical path. The physical path consists of layout generation and verification. Layout generation has reported to cause nearly 30% deviation of the electrical results in small nodes (20 nm and below). Hence, it is of very critical importance to seek automation solutions for the layout generation problem.

The thesis is divided into five chapters in addition to the lists of contents, tables and figures as well as list of references and one appendix.:

- Chapter 1: Introduction to Analog Circuit Layout Generation
 - Presents a brief introduction to the area of analog IC design automation, with special emphasis to the automatic layout generation.
- Chapter 2: Literature Review on the-State-of-the-Art Solutions
 - Present the placement and routing problem in the EDA and a brief overview of the most recent tools developed in this field.
- Chapter 3: Proposed Automation Flow
 - Gives an overview of the proposed automatic flow for analog IC design, with emphasis on the layout generation task
- Chapter 4: Results & Discussions
 - The flow will be demonstrated on a differential operational transconductance amplifier "OTA"
- Chapter 5: Conclusion & Future Work

Key words: Analog Layout, Automation, Analog Constraints, Integrated Circuits, Placement, Matching, Satisfiability Modulo Theories, Analog Routing.

Acknowledgment

First and foremost, I would like to thank God Almighty for giving me the strength, knowledge, ability and opportunity to undertake this research study and to persevere and complete it satisfactorily. Without his blessings, this achievement would not have been possible.

I would like to express my sincere gratitude to my advisor Prof. Dr. Mohamed Dessouky for the continuous support of my study and research, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis.

Also, I would like to thank my colleagues Sherif Ahmed and Soha Hamed for their continues discussion and team work to finish this research.

I appreciate and thank Sherif Saif, Islam Nashaat, Wael Abdallah, Mohamed Omar Darwish and Ahmed Arafa for their caring friendship, encouragement and help especially during the final stages of my thesis. My sincere thanks to my team in SI-Vision for their discussion and suggestions.

Finally, my deep and sincere gratitude to my family for their continuous and unparalleled love, help and support. I am grateful to my brothers for their support and encouragement. I am forever indebted to my parents for giving me the opportunities and experiences that have made me who I am, I owe my deepest gratitude to my wife, Dr Sarah Magdy, for her affection, encouragement, understanding and patience. She supported me without any complaint or regret that enabled me to complete my M.Sc thesis, and special thanks to my son Omar.

Thanks also to anyone I've forgotten who was instrumental in this project.

February 2020

Contents

STATEMENT	3
RESEARCHER DATA	4
ABSTRACT	5
THESIS SUMMARY	6
ACKNOWLEDGMENT	7
CONTENTS	8
LIST OF FIGURES.....	12
LIST OF TABLES	15
ABBREVIATIONS.....	16
CHAPTER 1 INTRODUCTION.....	17
1.1 ANALOG AND MIXED SIGNALS (AMS) ICS.....	17
1.2 ANALOG CIRCUITS LAYOUT GENERATION AND VERIFICATION	21
1.3 MOTIVATION FOR ANALOG DESIGN AUTOMATION	25
1.4 ANALOG LAYOUT AUTOMATION	27
1.5 ADVANCES TO STATE-OF-THE-ART	28
1.6 CONCLUSION	30
CHAPTER 2 AUTO-PLACEMENT AND ROUTING SURVEY.....	31

2.1 PLACEMENT.....	32
2.1.1 Analog Topological Constraints.....	32
2.1.2 Floorplan Representations.....	33
2.1.2.1 Absolute Representation	34
2.1.2.2 Topological Representations	35
2.1.2.2.1 Slicing Representations.....	36
2.1.2.2.2 Non-Slicing Representations.....	37
2.1.3 Modern analog placement challenges and schemes.....	40
2.1.3.1 Pareto Front of Placement Solutions	40
2.1.3.2 Thermal-Driven Placement.....	42
2.1.3.3 Current-Driven Placement	42
2.1.4 Stochastic Optimizer.....	43
2.1.5 Commercial Solutions	43
2.2 ROUTING	44
2.2.1 From Netlist to Pathfinder	44
2.2.2 Electromigration and IR-drop	45
2.2.3 Electromigration-Aware Approaches	45
2.2.4 Wiring Symmetry.....	46
2.2.5 Routing algorithms.....	46
2.3 ANALOG LAYOUT ALGORITHMS CLASSIFICATIONS	49
2.3.1 Procedural algorithms.....	50
2.3.2 Template algorithms.....	50
2.3.3 Optimization algorithms	50
2.4 COMPLETE LAYOUT GENERATION TOOLS	51
2.5 SUMMARY.....	55

CHAPTER 3 PROPOSED AUTOMATION FLOW	57
3.1 PATTERN GENERATOR & PHYSICAL ASPECT RATIO ESTIMATION	60
3.1.1 Common Centroid Matching	60
3.1.2 Interdigitization Matching	65
3.2 AUTOMATIC ROUTER OF CURRENT MIRROR.	66
3.2.1 Placing the gates contacts	68
3.2.2 The implant extension.....	69
3.2.3 Sources and drains metal extension and adding vias	70
3.2.4 Bulk connections.	71
3.2.5 Gates global routing	72
3.2.6 Drains local routing.....	73
3.2.7 Drains global routing	74
3.2.8 Placing Metal VIAS.....	76
3.2.9 Verification.....	77
3.3 AUTOMATIC ROUTER OF DIFFERENTIAL PAIRS.....	78
3.4 TOP LEVEL ROUTER TOOL.....	79
3.4.1 Global Router	80
3.5 SUMMARY.....	90
CHAPTER 4 RESULTS AND DISCUSSIONS	91
4.1 PARSER TOOL	91
4.2 SCHEMATIC RECOGNIZER.....	92
4.3 PLACEMENT AND ROUTING ESTIMATION	92
4.4 SMT PLACER.....	95
4.5 PHYSICAL PLACEMENT	98

4.6 BUILDING BLOCK ROUTER	98
4.7 SUMMARY AND DISCUSSION.....	99
CHAPTER 5 CONCLUSION AND RECOMMENDATION FOR FUTURE WORK	101
REFERENCES	104
AUTHOR’S PUBLICATIONS	111
APPENDIX.....	112

List of Figures

Figure 1-1: AMS Design flow (5).	19
Figure 1-2: Layout generation and verification process flow.....	21
Figure 1-3: (Upper) current mirror layout & (bottom) differential pair layout.....	25
Figure 1-4: Sample result from Plantage (source [7]).	29
Figure 2-1: Common topological constraints. A) Symmetry, B) Matching pattern, and C) Proximity. 33	
Figure 2-2: Layout example and its representation is slicing tree.	36
Figure 2-3: Non-slicing topology example known as wheel.....	37
Figure 2-4: Example of topological layout representations a) Placement with two symmetry.....	38
Figure 2-5: Comparison between traditional shape function (above) and enhanced shape function (below).	42
Figure 2-6: The Maze router algorithm	47
Figure 2-7: Line expansion routing algorithm.	48
Figure 2-8: SMT and MRST routing algorithms.	49
Figure 2-9: Chronological representation of analog layout generators	55
Figure 3-1: Proposed analog layout tool automation	59
Figure 3-2: Quarter cell approach.....	60
Figure 3-3: The cross-quad technique.....	61
Figure 3-4: Quarter cell generated by the tool's algorithm.	62
Figure 3-5: Half-cell generated by the tool's algorithm.	62
Figure 3-6: Full array generated by the tool's algorithm.....	63