AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
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Electronics and Communications Engineering Department

Design and Implementation of the RF Transceiver for LTE User Equipment.

A thesis submitted in partial fulfilment of the requirements of the degree of Doctor of Philosophy in Electrical Engineering

Submitted by

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Statement of Original Authorship

This thesis is submitted as a partial fulfilment of Doctor of Philosophy degree in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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ABSTRACT

CMOS processes have become more and more popular for radio-frequency integrated circuit (RFIC) design due to its cost effectiveness, high noise immunity, low power consumption and compatibility with the silicon based system on chip (SOC) technology. CMOS is a suitable choice for the transceiver design including power amplifiers, modulator and demodulator, and voltage controlled oscillators. The primary considerations in transceiver architecture design are complexity, cost, size, power dissipation and the number of external components. LTE transceiver can be divided into two major parts: the baseband part and the RF part. Typically, the baseband part is mostly implemented in the digital domain while the RF front-end part is an analog part. A digital to analog converter (DAC) and an analog to digital (ADC) converter are the interface connecting the baseband and RF sections.

This dissertation introduces the analysis and design of RF front-end of LTE transceiver that includes RF Power amplifier, I/Q (De-) Modulator, and quadrature voltage controlled oscillator in 130 nm CMOS technology. The investigated PA, I/Q modulator and demodulator, and VCO are analyzed, simulated, and designed using software packages as (Advance Design System (ADS), Cadence Design Systems and Ansoft High Frequency Structure Simulator (HFSS)). Verification of the designs are done through comparison between the simulated results and the recently reported designs.

Firstly, a multi-bands multi-mode Class-AB/F power amplifier (PA) is proposed to cover 0.1- 4.2GHz band and suitable for multi-standard applications. The proposed PA can operate in linear mode (class-AB) for variable-envelope modulated signals and switching mode (class-F) for constant-envelope modulated signals. The proposed PA has off-chip inter-stage and output matching networks over the specified frequency band, while the input stage is Complementary Current-Reuse common-gate with active shunt feedback configuration to achieve

Ultra-Wideband (UWB) input matching and save power consumption. Class-AB PA has a saturated output power of 23.5 dBm ±1 dB over 0.1-4.2GHz, a power-added efficiency (PAE) of 41 %, a third order intercept point (OIP3) of 17 dBm, and adjacent channel power ratio (ACPR) of -29.3dBc for LTE 15MHz channel bandwidth. The maximum PAE of 62.1% under the class-F operation is achieved at 24.5-dBm output power. The PA occupies 0.64 mm^2 of active chip area, while the estimated off-chip area is 13.3 mm^2. The proposed PA consumes 164 mW, and 16 mW in class-AB and class-F, respectively.

Secondly, ultra-wideband (UWB) in-phase/quadrature (I/Q) demodulator, and reconfigurable wideband (I/Q) modulator are presented for multi-standard applications. The proposed designs can be used in multi-band or wideband LTE RF transceiver. Both the RF stage in the demodulator, and the IF stage in the modulator are implemented using Capacitive Cross Coupling (CCC) common-gate configuration to enhance bandwidth and increase gain. Furthermore, a high coupling wideband five port transformer with coupling coefficient (K) of 0.8 is designed using 3D High Frequency Structure Simulator (HFSS) to achieve wideband output matching with less occupied chip area in the modulator. The demodulator consumes 10.5 mW from 1.2 V supply and it has conversion gain (CG) of 10 dB with 3-dB bandwidth of 9 GHz (1-10GHz). The demodulator input 1-dB compression point (P1dB) is -4.15dBm at 4.5 GHz, and LO-to-RF isolation is better than -45 dB due to compact and fully symmetrical layout where the active area is 0.22mm^2. The modulator demonstrates CG of 6.8±1.5 dB in the frequency band 1.5-4 GHz, where the maximum CG equals 8.32dB at LO power 3dBm, and OP_1dB equals -1.6 dBm. Also, the LO suppression and the harmonic suppression in the modulator are better than -50dBc, and -60dBc, respectively. The modulator active area is 0.55mm^2 and the power consumption is 16.6mW from 1.2 V supply.

Finally, a 0.35mW Class-C series coupling quadrature voltage-controlled power oscillator (S-QVCO) based on the coupling between two identical LC VCOs is presented for multi-standard applications. The proposed QVCO achieves tuning range of 28.2% from 2.3 to 3.07 GHz, and low phase noise of -119.2 dBc/Hz at a 1-MHz offset frequency from 2.7 GHz carrier. By biasing the proposed QVCO in class-C, the drawn current is reduced from 1.48 mA to 0.35 mA compared to the class-B counterpart from 1V supply voltage. The minimum achieved Figure-of-Merit (FOM) equals -192 dBc/Hz and the maximum given output power is 6.5 dBm. The phase error between the quadrature output signals is at most 0.25° .The active area of the proposed QVCO equals $0.34\ mm^2$, while the total chip area including RF pads is $1\ mm^2$.

Keywords: Capacitive cross coupling; Class-AB/F ; Class-B; Class-C; CMOS; Conversion gain; Coupling coefficient; Demodulator; Down-conversion; FoM; LC-Tank; Mixer; Multi-mode; Phase error; Phase noise; Power Amplifier (PA); Quadrature Q-factor; Radio Frequency (RF); Reconfigurable; RF transceiver; RF Transmitter; Up-conversion; Voltage-controlled oscillator.

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