بسم الله الرحمن الرحيم

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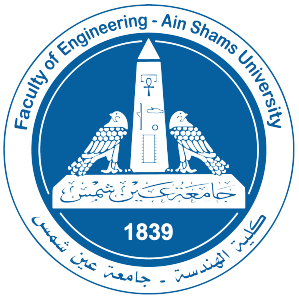
تم رفع هذه الرسالة بواسطة /صفاء محمود عبد الشافى

بقسم التوثيق الإلكتروني بمركز الشبكات وتكنولوجيا المعلومات دون أدنى مسئولية عن محتوى هذه الرسالة.

ملاحظات: لايوجد



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Computer and Systems Engineering Department

Intelligent Techniques for Model Order Reduction

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Computer and Systems Engineering)

by
Nourhan Essam Ahmed Shiba El-Hamd
Bachelor of Science in Electrical Engineering
(Computer and Systems Engineering)
Faculty of Engineering, Ain Shams University, 2017

Supervised By
Prof. Dr. Mohamed Watheq Ali Kamel El-Kharashi
Dr. Cherif Ramzi Salama Andraos Kozman Salama

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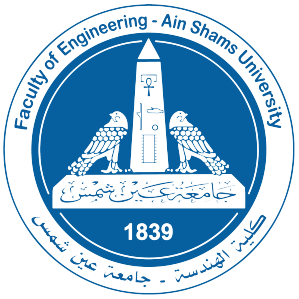

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Examiners' Committee

Name and affiliation	**Signature**
Prof. Dr. Hassanein Hamed Amer Professor, Electronics and Communications Engineering Department The American University in Cairo.	.....
Prof. Dr. Ashraf Mohamed El-Farghaly Salem Professor, Computer and Systems Engineering Department Faculty of Engineering, Ain Shams University.	.....
Prof. Dr. Mohamed Watheq Ali Kamel El-Kharashi Professor and Chair of Computer and Systems Engineering Department Faculty of Engineering, Ain Shams University.	.....

Date: 24 February 2022

Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Nourhan Essam Ahmed Shiba El-Hamd

Signature

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Date: 24 February 2022

Researcher Data

Name: Nourhan Essam Ahmed Shiba El-Hamd
Date of Birth: 15/09/1994
Place of Birth: Mecca, Saudi Arabia
Last academic degree: Bachelor of Science
Field of specialization: Computer and Systems Engineering
University issued the degree : Ain Shams University
Date of issued degree : 2017
Current job : Senior Software Development Engineer at Siemens

Abstract

Circuit simulation has always been a crucial step in system design and verification. A chip design has to be simulated multiple times to verify that it is properly operating. To ensure the reliability of the design flow, RC parasitic effects are extracted at the interconnect structures and accounted for during simulation. The advanced technologies and continuous scaling are resulting in designs becoming more complex and dense. Real chip designs usually have huge parasitic networks which lead to very expensive, or even intractable, simulation. This increasing cost gave rise to the need for efficient techniques capable of improving the simulation run-time and providing a higher system capacity. One such technique is Model Order Reduction (MOR).

MOR is applied on circuits so that, instead of simulating the circuit's complex model, computation efforts are reduced by simulating a simpler version of it. This model simplification is achieved by reducing the parasitic networks while preserving the circuit's essential properties as well as the terminals specified by the designer. Even though MOR reduces the system's complexity, the full reduction of networks having many terminals often results in a smaller dense network instead of a large sparse one. The high density of the resulting network might, in fact, slow down the simulation.

This thesis contributes a novel dense sub-circuit reduction system where the system uses dense sub-graph mining techniques on top of MOR techniques. The proposed has the advantage of being integrated with any MOR technique for circuit reduction as well as any dense sub-graph mining technique. Our work also does a comparative analysis between four dense sub-graph mining algorithms in the context of circuit reduction. The comparison showed that the greedy approximation algorithm for edge density maximization is recommended to be applied on the circuit reduction problem since it has good results in terms of the density of the detected sub-graph, the size of the detected sub-graph, and the scalability of the system on large networks.

To assess the effectiveness of our proposed work, the developed approach was integrated with a commercial tool and tested on real-world designs. It was further evaluated against TICER, a commercial reduction tool, to provide a fair comparison. The results prove the success of our work in reducing the dense sub-circuits in timely manner. The results show improvement in the circuits' sparsity. Additionally, the results show enhancements in some reduction and simulation aspects.

Summary

In large VLSI process nodes, the designs are considered to be ideal since the effect of interconnect structures between the devices is minimal. With the increasing speed and density of circuits and the shrinking of technologies, the mutual effects between the interconnect structures are becoming more significant thereby, resulting in designs becoming less ideal. Moreover, the delay resulting from the interconnect structures is becoming progressively more dominant in the overall circuit delay. Thus, it became indispensable to account for the parasitic effects of the wiring or interconnect structures. The parasitic effects, while improving modeling accuracy, result in huge designs that might outpace the capacities of simulators. In order to have simulatable designs while accounting for the parasitic effects, the circuit has to be reduced into a simpler form that preserves its essential properties. Thus, instead of simulating the circuit's complex model, the simpler version is simulated. The aforementioned reduction process is formally known as model order reduction (MOR). MOR techniques for circuit reduction are capable of reducing circuits while preserving the user-defined terminals as well as the essential properties. It is evident that MOR improves the simulation run-time and provides a higher system capacity. However, when networks have many terminals, their full reduction often results in a small dense network rather than a large sparse. Having dense networks might slow down the simulation. This is because simulation is based on solving some matrices representing the system and dense matrices, despite having fewer unknowns, have more elements than sparse ones. In this work, we focus on improving some reduction and simulation aspects by reducing the dense sub-circuits while leaving the sparse ones unaltered. The system is built upon preexisting MOR techniques. The proposed system also represents the circuit using the graph representation and uses graph theory in order to find the dense sub-graphs in the large circuit graph. At first, we conducted a comparative analysis between four dense sub-graph mining algorithms in the context of circuit reduction. The comparison showed that the greedy approximation algorithm for edge density maximization is recommended to be applied on the circuit reduction. The proposed system was then built using C++ programing language and was integrated inside Calibre PEX which is a commercial EDA tool for parasitic extraction and reduction. We measured various reduction and simulation aspects and compared the system with TICER which is a commercial MOR tool used inside Calibre PEX. Additionally, we created some Python scripts to properly evaluate the system and used ELDO simulator. This thesis is organized as follows:

The thesis is divided into eight chapters as listed below:

Chapter 1: Introduction:

The chapter discusses the importance of circuit simulation and model order reduction. It also gives a quick introduction about dense sub-circuits effect on the simulation. The chapter also presents the main research objectives.

Chapter 2: Background:

The chapter provides the background necessary to understand the rest of the thesis is briefly discussed. The chapter gives a detailed overview about the EDA concepts and the parasitic extraction process. Circuit structure and representation are also presented. Moreover, MOR is extensively studied in this chapter.

Chapter 3: Problem Formulation and Related Work:

The problem that this thesis is focusing on is stated and formulated in this chapter. Various enhancement aspects where discussed. Additionally, various design approaches were presented with their advantages and disadvantages.

Chapter 4: Proposed Approach:

The proposed approach is clearly stated in this chapter along with the different modules and tools used.

Chapter 5: Dense Sub-Circuit Reduction:

This chapters discusses the problem of dense sub-graph mining and how it can be used in the context of circuit reduction. The chapter describes some algorithms used in dense sub-graph mining as well.

Chapter 6: Evaluation of Dense Sub-Circuit Reduction:

In this chapter, a comparative analysis of different dense sub-graph mining was performed in the context of circuit reduction.

Chapter 7: Evaluation of Proposed Approach:

The full proposed approach is evaluated to assess our work against other commercial tools.

Chapter 8: Conclusion and Future Work:

This chapters draws the conclusions of the thesis along with potential future work based on the findings and observations made.

Keywords: computer-aided design, dense sub-graph mining, graph algorithms, graph mining, integrated circuit simulation, model order reduction, RC circuit reduction, RC circuits, scalability, VLSI