AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

ELECTRONICS AND COMMUNICATIONS ENGINEERING

Large Scale Circuit Analysis: An Analog signature-based partitioning approach

A Thesis Submitted in partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Mechanical Engineering

by

Sherif Hany Riad Mohammed Mousa

M.Sc. of Electrical Engineering

(Electronics and Communication Engineering)

Faculty of Engineering, Ain Shams University, 2013

Supervised by

Prof. Dr. Hani Fekri Ragai

Prof. Dr. Emad Eldin Mahmoud Hegazi

Cairo – 2022

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Cairo - 2022

STATEMENT

This thesis is submitted as partial fulfillment of Doctor of Philosophy in Electrical engineering, Faculty of Engineering, Ain Shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Sherif Hany Riad Mohammed Mousa

Signature

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Date: / / 2022

Researcher Bio

Sherif Hany Mousa Sherif is a senior IEEE member. He received both his B.Sc. and M.Sc. degrees in electrical and communication engineering from Faculty of Engineering Ain-shams University in Egypt in 2007 and 2013 respectively. Currently, he is perusing his Ph.D. in the same university in the field of structural techniques for analog design for testability and circuit analysis. On the professional level, Sherif is assuming the role of a Principal Technologist in the Calibre Design Solutions division of Siemens EDA, a part of Siemens Digital Industries Software. Since 2007, Sherif held several positions as a technical marketing engineer, Calibre product engineer, analog quality assurance engineer as part of ChameleonART, and IC design consultant for physical, circuit and reliability verification flows as well as analog/mixed signal applications. He has authored multiple publications and holds multiple patents in the fields of analog layout porting, DFM, hotspot detection and correction, and machine learning-assisted verification flows.

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Date of issued degree	2013

Publications

1. S. Hany, E. Hegazi, and H. F. Ragai, "SALAH: Simulation-Assisted LAyout Hierarchy Construction," 2021 22nd International Symposium on Quality Electronic Design (ISQED), 2021, pp. 312-312, doi: 10.1109/ISQED51717.2021.9424317.

2. S. Hany, Shohdy Abdel Kader, H. F. Ragai, and E. Hegazi. "Improving the system thermal reliability using thermal-gradient-based placed heaters." 2020 Journal of Green Engineering, volume 10, issue no. 12, pp. 13743-13753, ISSN: 2245-4586.

3. S. Hany, H. F. Ragai and E. Hegazi, "ANtarctica: ANalog Thermal Aware, with Reduced Constraint, Technique for Checking & Analysis," 2020 IEEE International Integrated Reliability Workshop (IIRW), 2020, pp. 1-4, doi: 10.1109/IIRW49815.2020.9312856.

Summary & Contents

VLSI design and fabrication process requirements are evolving specially when it comes to turn-around time, quality of results and the associated database size. Traditional database optimization techniques aim at leveraging database parallel processing. However, the input database optimization is still lagging due to dependency on the geometrical aspect of the design without leveraging its electrical front-end counterpart. Moreover, some design stages such as thermal verification requires a database that consolidates geometrical, electrical, and thermal data.

Thermal analysis and verification of SoCs have become critical steps in IC design cycle from the reliability aspect for most of the design types. Commercial and traditional mechanisms are known to be slow, complex, and indicate the fixes very late in the design cycle with a big focus on the packaging level and a relatively small focus for the design analog back-end layouts which is critical for applications such as Automotive, 5G, and IoT.

This thesis demonstrates a new thermal verification flow that leverages an electrical-aware data mining scheme. The proposed scheme constructs an optimized database by adopting an electrical signature to drive the database partitioning-clustering mechanism. The optimized database contains electrical-aware data clusters that eliminate redundancy hence improve runtime, accuracy, and allow for extended validation for analog sensitivity, matching, and compliance with reliability guidelines such as identifying thermal hotspots, verifying thermal symmetry and thermal gradient.

The proposed verification flow has been used to drive interactive thermal hotspots fixing in early design phases. With the objective of reducing the peak thermal/power density in hotspots and achieving thermal symmetry, the flow allows optimizing heat source locations across the chip extent.

The proposed flow permits benefits that can be readily realized as it provides fast, interactive, and actionable feedback to optimize the placement of the critical devices. The flow has been proven on small as well as large scale analog designs covering turn-around time (TaT), ease of use (EoU), and quality of results (QoR) aspects. The results have been compared to the state-of-the-art techniques and results from designs with same complexity and size.

The thesis is organized in five chapters as follows:

Chapter one demonstrates the significance of the study, its objective, motivation, and research contribution. The chapter starts by covering the design to tape-out cycle requirements and challenges regarding TaT, EoU, and QoR. It then covers the growing importance and the need for thermal analysis as well as the associated analog requirements for thermal symmetry and thermal gradient checking.

Chapter one also shows real-life examples from the industry about the growth of database size and complexity. This chapter lays the ground for the scope of the study covering main assumptions, boundary conditions, and aligns/maps the used concepts to other disciplines of big data and machine learning.

Chapter two reviews the literature covering the role of partitioning across different design phases and narrows it down later to traditional thermal analysis mechanisms. The chapter walks through the philosophy of each mechanism and its weaknesses in a comparison to others. The covered mechanisms vary from the most common post-silicon thermal checking to the recent pre-silicon ones before it narrows down the discussion to thermal verification flows in a functional-based mechanism. Finally, the chapter introduces an electrical signature-based partitioning and clustering concept that is incorporated in the proposed thermal/power verification flow.

Chapter three provides an overview for the proposed thermal verification methodology. It extends the signature-based partitioning-clustering concepts in context of database construction with a focus on improving database accuracy by identifying more topologies and removing redundancies as well as assisting in thermal hotspot identification and conducting advanced thermal checking. Chapter 3 provides pseudo codes and concepts for the newly introduced parts regarding building heatmap, thermal verification mechanism as well as the various fixing solutions.

Chapter four highlights the research findings, observations, and implications of applying the signature-based partitioning-clustering database construction approach on different sized testcases and designs. The results are evaluated for unit test structures with focus on accuracy and QoR. Then the flow is applied on real analog design scenarios; a ring-based voltage-controlled oscillator (VCO) and a low noise amplifier (LNA) to show the runtime savings as well as the heatmap and the identified hotspots. The generated heatmaps and the incorporated reliability checks are then used to drive advanced checking and fixing solutions that aim at identifying thermal hotspots as well as improving thermal symmetry and thermal gradient.

Chapter five concludes the research by summarizing the new incorporated signatures in creating an electrical-aware database as well as a new approach of early evaluation of thermal hotspots, thermal symmetry mismatches, and thermal gradient violations. It emphasizes the impact of the proposed flow in ensuring compliance to reliability guidelines specially for analog blocks. Finally, the chapter highlights the achieved goals of the study and recommends future research points and directions.

Abstract

VLSI thermal analysis and management mechanisms have become more critical for SoCs performance and yield. Especially with the growing complexity in design requirements and manufacturing process, more physical, circuit and reliability checks are needed to accomplish tape-out with faster turn-around time (TaT) and better quality of results (QoR). Thermal issues are more commonly manifested as soft/out-of-specification failures. Not only these soft failures tend to alter the carrier mobility, clock timing delays, leakage power and electrical matching requirements, but also it creates reliability issues such as mean-time-to-failure (MTTF) and aging phenomenon such as bias temperature instability, time-dependent dielectric oxide breakdown, and electromigration.

Traditional thermal/power analysis mechanisms started as post-silicon point-contact thermocouple or infrared imaging processing that took place on the fabricated chip specially on the packaging level which do not give actionable feedback to the designers. This led to a very expensive thermal fixing and controlling mechanisms of reimplementing the whole design in an iterative process. Pre-silicon thermal analysis mechanisms are either design-, placement-, or electrical-based techniques: design-based techniques, such as clock and power gating, are digital domain oriented and usually require bulky on-chip thermal control circuits. Placement-based techniques are not standardized and tied to specific design environments while the electrical-based techniques provide early and actionable feedback to designers.

The challenges in the electrical-based thermal analysis are not only related to the complex electrothermal modeling, but also that they need larger database that consolidates geometrical, electrical, and thermal information. Advanced database management and parallel processing techniques are continuously evolving to cope with the exponential growth in data size. However, it is essential to optimize the input data itself by pivoting on the VLSI aspects. This gives rise to the need to design, simulate and verify the whole system after decomposing (partitioning) it into smaller subsystems and rebuilding its database bottom-up (clustering) based on optimized and electrical-aware data. Various partitioning-clustering mechanisms are invoked for every design phase. Iterative graph-based partitioning mechanisms used in circuit simulators have low parallelization capabilities. On the other hand, cell-based (hierarchical/agglomerative), template-based (clip/density) and pattern-based partitioning mechanisms scale better on multiple threads, but they are limited to geometrical processing such as design rule checking and lithography simulations respectively. Recent partitioning mechanisms use functional- and electrical-driven partitioning to fulfill advanced verification requirements.

This work proposes a new thermal verification flow that leverages an electrically aware partitioning-clustering data mining scheme. This scheme adopts a signature-based approach for database optimization inspired by analog DFT signature techniques. The proposed flow demonstrates the database compression QoR, EoU and TaT of a low noise amplifier block. Moreover, it allows for extended reliability checks which are later used to drive a thermal management technique that allows for resolving thermal hotspots, thermal symmetry mismatches, and smoothens the thermal gradients. The results are compared to the state-of-the-art techniques in literature on blocks with similar size and complexity.

Keywords: Reliability verification, Thermal-aware layout analysis, thermal hotspot detection, thermal symmetry, thermal matching, thermal gradient, isothermals, heatmap, thermal profile, database size, electrical signature, supply ramping, partitioning, clustering, physical verification, design profiling, topological patterns, failure analysis, design for manufacturability, analog DFT, power scan chain, thermal fixing.

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By the time of defending this thesis, we have lost Dr. Emad Hegazi who represented a lot more for me beyond just being an amazing professor, scholar, and scientist. He has been a big brother, a friend, and a role model who I aspire to raise to his reputation and achievements.

My relationship with Dr. Emad had started with several undergraduate courses in analog electronics before I collect my courage and ask him to be my supervisor. Since then, Dr. Emad lured me to do my postgraduate studies. He managed to keep me excited, engaged, and continue working on both my M.Sc. then Ph.D. both in parallel to a full-time life (not only job but marriage, relocating to a different country, having kids). Of course, it has been a tiring journey, but I could not have done it without his flexibility, understanding, and support. During more than 12 years, Dr. Emad kept calling, messaging, and contacting me on weekly basis to get an update, pass a new piece of info, propose an exciting new idea on ideas such as how to not be limited to just a thesis to have a book, introduce the concept in courses, offer extensions and learning opportunities as a graduation project, build a core of a new EDA company, … etc. Working with Dr. Emad gave me a long-term purpose to invest in my career and envision how I can invest in and return to my beloved country, Egypt.

These research opportunities helped me advancing in my career and evolve even on the personal level. He has always talked about his beloved family and his philosophy in raising his student kids and his real kids and how he is always exploring and trying new sports, have targets in learning a new piece of music “Turkish march”, read a new book, … etc. He was very good at injecting cultural aspects and knowledge to his projects by naming them after musicians (using their first names) or using advanced vocabularies. He was amazed when I started to pick up some of such learnings and divided my Ph.D. thesis into two flows once of them named after Mohamed Salah (**M**echanism of **S**imulation-**A**ssisted **L**ayout p**A**rtitioning and Analysis of **H**otspots).

Dr. Emad would be missed but he will always live in our hearts, our work, in the knowledge that he passed to thousands of students, and his investments in building Egypt. May Allah reward him and count those acts as righteous deeds.

إِذَا مَاتَ الإِنْسَانُ انْقَطَعَ عنْه عَمَلُهُ إِلَّا مِن ثَلَاثَةٍ: صَدَقَةٍ جَارِيَةٍ، أَوْ عِلْمٍ يُنْتَفَعُ بِهِ، أَوْ وَلَدٍ صَالِحٍ يَدْعُو له.

List of Abbreviations

1D/ 2D/ 3D	One/two/three dimensions
3DIC	Three-Dimensional integrated circuit packaging
ACLV	Across-chip length variation
ADC	Analog-digital-converter
AI	Artificial intelligence
AMF	Absolute mismatch factor
AMS	Analog mixed signal
AWS	Amazon web services
ANtartica	ANalog Thermal Aware, with Reduced Constraint, Technique for Checking & Analysis
ATE	Automatic test equipment
ATPG	Automatic test pattern generator
BCI	Boundary Condition Independent
BEOL	Back-end of line
BICI	Boundary and Initial Condition Independent
BTI	Bias Temperature Instability -refer to PBTI and NBTI
CAD	Computer aided design -refer to EDA
CBC	Correct-by-construction
CDF	Cumulative density function
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical mechanical polishing
CPU	Central processing unit
CTAT	Complement to absolute current -refer to PTAT
CTM	Compact thermal model -refer to DTM
CUT	Component under test
CV	Circuit verification
DB	Database
DC	Direct current -refer to DC OP
DC OP	DC operating point
DEF	Design exchange format -refer to LEF
DFM	Design for manufacturability
DFT	Design for testability
DFX	Design for excellence or design for variable X
DoF	Degree of freedom
DP	Double patterning -refer to MP
DRC	Design rule check

DTM	Detailed thermal model -refer to CTM
ECO	Engineering change order
EDA	Electronic design automation
EM	Electro-migration
EoS	*Electrical over stress*
ERC	Electrical rule check
ESD	Electrostatic discharge
EUV	Extreme ultraviolet
FEM	Finite element methods
FEOL	Front-end of line -refer to BEOL
FET	Field effect transistor
FoM	Figure of merit
FTDT	Finite Difference Time Domain
GAA FET	Gate-all-around FET
GB	Giga bytes
GHz	Giga Hertz
HCI	Hot Carrier Injection
HDB	Hierarchical database
HDL	Hardware description language
HP	High power
HV	High voltage
HZ	Hertz -refer to GHZ
IDDQ	Drain supply quiescent current
IGBT	Insulated-gate bipolar transistor
I/O or IO	Input/output
IoT	Internet of things
IR	Ohmic voltage drop (I is current and R is resistance)
LDO	Low-dropout regulator
LED	Light emitting diode
LEF	Library exchange format - refer to DEF
LNA	Low noise amplifier
LP	Low power
LPF	Low pass filter
LSB	Least significant bit
LUT	Look-up table
LV	Low voltage
LVS	Layout-versus-schematic
MC	Monte Carlo