بسم الله الرحمن الرحيم

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تم رفع هذه الرسالة بواسطة / سامية زكى يوسف

بقسم التوثيق الإلكتروني بمركز الشبكات وتكنولوجيا المعلومات دون أدنى مسئولية عن محتوى هذه الرسالة.

ملاحظات: لا يوجد

EFFICIENT HIGH LEVEL SYNTHESIS IMPLEMENTATION FOR DEEP CONVOLUTIONAL NEURAL NETWORKS ON FPGA

By

Muhammad Nabil Muhammad Sarg

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Title of Thesis:
Efficient High Level Synthesis Implementation for Deep Convolutional Neural Networks on FPGA

Key Words:
Convolutional Neural Network; Field Programmable Gate Array; Hardware Accelerator; High-Level Synthesis

Summary:
Deep Convolutional Neural Networks (CNNs) play an important role in computer vision applications. However, they are computational-intensive and resource-consuming. Thus, it is hard to integrate them into embedded platforms. The FPGA is one of the most promising platforms for accelerating Deep CNNs due to its configurability, high-performance, low power, and shorter development cycles. In this research, we introduce a diverse High Level Synthesis (HLS) C++ Deep CNNs compiler that generates highly efficient implementation for accelerating the inference task of Deep CNNs on FPGAs. We developed HLS C++ implementations for the Deep CNNs blocks that efficiently utilizes the FPGA available resources to achieve the maximum inference performance. The developed compiler automates the customization of the accelerator HLS implementation to best fit the selected Deep CNN model. The proposed work is demonstrated with an implementation of two different Deep CNN models, Resnet-50 and VGG16, on Xilinx Zynq MPSoC using SDSoC development environment.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Muhammad Nabil Muhammad Sarg Date: ../ ../2022

Signature: Muhammad Nabil Muhammad Sarg

Dedication

To my parents, my wife, and my little child.

Acknowledgments

I would like to offer my sincere thanks to my supervisors Prof. Ahmed Hussien and Dr. Hassan Mostafa. I'd want to convey my heartfelt thanks to Dr. Hassan for his invaluable guidance, encouragement, and active assistance during this project.

My heartfelt thanks and love to my family for their support and encouragement.

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Nomenclature

AI	Artificial Intelligence
ANN	Artificial Neural Networks
ASIC	Application-Specific Integrated Circuit
BN	Batch Normalization
BRAM	Block Random Access Memory
CNN	Convolutional Neural Network
CPU	Central Procession Unit
DL	Deep Learning
DRAM	Double Random Access Memory
DSP	Digital Signal Processing
FC	Fully Connected
FPGA	Field-Programmable Gate Array
GPU	Graphical Procession Unit
HLS	High-Level Synthesis
IFMAP	Input Feature Map
LUT	Look Up Table
MAC	Multiply and Accumulate
MPSoC	Multi Programmable System on Chip
OFMAP	Output Feature Map
RTL	Register Transfer Logic
URAM	Ultra Random Access Memory