بسم الله الرحمن الرحيم

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تم رفع هذه الرسالة بواسطة / حسام الدين محمد مغربي

بقسم التوثيق الإلكتروني بمركز الشبكات وتكنولوجيا المعلومات دون أدنى مسئولية عن محتوى هذه الرسالة.

ملاحظات : لا يوجد

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications Department

Hyprid Analog-to-Digital Converter for Low Power Applications

A Thesis submitted in partial fulfillment of the requirements of
the degree of Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications Department)

by
Ali Ahmed Badawy AbdelRazek
Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2014

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Cairo, 2022

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electronics Engineering and Electrical Communications Department, Faculty of Engineering, Ain shams University.

The author implemented the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Noise Shaping Successive-Approximation Analog-to-Digital Converters (NS SAR ADCs) are one of the most trending ADC topologies that are heavily researched in recent years. This high interest is attributed to the advantages of the NS SAR architecture that combines the merits of SAR and $\Sigma\Delta$ Converters. NS SAR ADCs are capable of achieving low power and high resolution at the same time. However, the implementation, of a NS SAR loop filter in a passive or active form, imposes some design challenges related to the power dissipation, technology scaling, performance, and robustness against PVT variations. The most critical block in a NS SAR ADC is the integrator that performs the residue integration. To obtain aggressive and accurate noise transfer function (NTF), a closed loop OTA can be used and will be power inefficient because of the static current consumed. It will be robust against PVT but it does not scale easily. A passive filter can be used instead but will give less aggressive NTF and will do less suppression to comparator noise as the passive gain is limited. Its gain will vary across PVT.

This thesis proposes an inverter-based NS SAR ADC implementation that alleviates these design challenges. This will keep the power efficiency of the integrator and will be scaled easily. The inverter-based OTA is self-tuned to achieve the required specs across PVT variation.

A system analysis of the different factors of a NS SAR ADC is performed showing the critical design specs and system design guidelines is set to ease the choice of NS filter. The proposed implementation is used to design a NS SAR ADC with cascaded FIR-IIR loop filter in 28-nm CMOS technology achieving an SNDR of 70.03 dB for an 11.25 MHz signal bandwidth, consuming 0.64 mW.

Summary

In this work, a noise-shaping successive-approximation register analog-to-digital converter (NS SAR ADC) is integrated with an inverter-based loop filter and presented thoroughly. This NS SAR ADC is robust against all process, voltage, and temperature (PVT) variations. It is also low power and serves best for low-power applications. It has an ease of technology scalability, as well. An analysis of the system design is explained along with the schematic designs of the building blocks. The simulation results are obtained and presented performing an overall performance of 12.1-bit ENOB with an 8-bit DAC array, OSR of 4, and SNDR of 70.03 dB consuming 0.64 mW and implemented on 28nm CMOS technology.

The thesis is divided into five chapters as listed below:

- Chapter 1: Introduction
  In this chapter, a quick introduction to the ADC and its modern applications is given. This chapter also explains what FOM is and introduces the different types of ADC including the SAR ADC, $\Sigma\Delta$ ADC and fianlly, the NS SAR ADC. At the end of this chapter, the organization of this document is briefly discussed.

- Chapter 2: State Of The Art Realizations
  This chapter discusses the state of the art for NS-SAR ADC. It has a defined comparison between this work and recent related publications. It shows the benefits and drawbacks of this work compared to the recent publications. It also illustrates the achievements of each paper and compares them and the specifications.

- Chapter 3: System-level design
  This chapter defines the system-level design for the proposed NS-SAR ADC. It includes all the equations used in this thesis and their derivations along with the measurements and simulation results to illustrate the whole process of having the desired output of the NS SAR ADC.

- Chapter 4: Design of an inverter-based NS SAR ADC in 28nm CMOS technology
  This chapter focuses on the analysis and design phase which includes the test bench setup and the required values and variables that are used in this thesis. It has a sufficient analysis to the design of the inverter-based NS SAR ADC in 28nm CMOS technology.

- Chapter 5: Conclusion
  Finally, this chapter summarizes the thesis and highlightes the main contributions. It also has some suggestions for future work for this thesis.

Keywords: Analog to Digital Converter (ADC), Effective Number of Bits (ENOB), Figure of Merit (FoM), Noise Shaping (NS), Sigma-Delta ($\Sigma\Delta$), Signal to Noise and Distortion Ratio (SNDR), Signal to Noise Ratio (SNR), Successive Approximation Register (SAR), inverter based, PVT tolerant, scaling friendly.

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