



بسم الله الرحمن الرحيم

∞∞∞∞

تم رفع هذه الرسالة بواسطة / سامية زكى يوسف

بقسم التوثيق الإلكتروني بمركز الشبكات وتكنولوجيا المعلومات دون أدنى

مسئولية عن محتوى هذه الرسالة.

ملاحظات: لا يوجد





# **AN INTEGRATED SIMULTANEOUS THERMAL AND RF ENERGY HARVESTING SYSTEM FOR WIRELESS SENSOR NETWORKS**

By

**Ahmed Abdulraouf Awad Ahmed Helaly**

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
in Partial Fulfillment of the  
Requirements for the Degree of  
**MASTER OF SCIENCE**  
in  
**Electronics and Communications Engineering**

FACULTY OF ENGINEERING ,CAIRO UNIVERSITY  
GIZA,EGYPT  
2022

# **AN INTEGRATED SIMULTANEOUS THERMAL AND RF ENERGY HARVESTING SYSTEM FOR WIRELESS SENSOR NETWORKS**

By

**Ahmed Abdulraouf Awad Ahmed Helaly**

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
in Partial Fulfillment of the  
Requirements for the Degree of  
**MASTER OF SCIENCE**  
in  
**Electronics and Communications Engineering**

Under the Supervision of

**Dr. Ahmed N. Mohieldin**

Professor

Electronics and Communications Engineering  
Faculty of Engineering , Cairo University

**Dr. Mohamed F. Abuelyazeed**

Professor

Electronics and Communications Engineering  
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING ,CAIRO UNIVERSITY  
GIZA,EGYPT  
2022

# **AN INTEGRATED SIMULTANEOUS THERMAL AND RF ENERGY HARVESTING SYSTEM FOR WIRELESS SENSOR NETWORKS**

By

**Ahmed Abdulraouf Awad Ahmed Helaly**

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
in Partial Fulfillment of the  
Requirements for the Degree of  
**MASTER OF SCIENCE**  
in  
**Electronics and Communications Engineering**

Approved by the Examining Committee:

---

<b>Dr. Ahmed N. Mohieldin,</b>	Thesis Main Advisor
--------------------------------	---------------------

---

<b>Dr. Mohamed F. AbuElyazeed,</b>	Thesis Advisor
------------------------------------	----------------

---

<b>Dr. Mohamed Yousef Abdallah,</b>	Internal Examiner
-------------------------------------	-------------------

---

<b>Dr. Sameh Assem Ibrahim,</b>	External Examiner
---------------------------------	-------------------

Professor  
Faculty of Engineering, Ain Shams University

FACULTY OF ENGINEERING ,CAIRO UNIVERSITY  
GIZA,EGYPT  
2022

**Engineer's Name:** Ahmed Abdulraouf Awad Ahmed Helaly  
**Date of Birth:** 04/06/1995  
**Nationality:** Egyptian  
**E-mail:** araouf@eng.cu.edu.eg  
**Phone:** 01010447316  
**Address:** First District, 6th of October, Giza, 12573  
**Registration Date:** 01/10/2018  
**Awarding Date:** --/--/2022  
**Degree:** Master of Science  
**Department:** Electronics and Communications Engineering



**Supervisors:**

**Dr. Ahmed N. Mohieldin**  
**Dr. Mohamed F. Abuelyazeed**

**Examiners:**

<b>Dr. Ahmed N. Mohieldin</b>	(Thesis Main Advisor)
<b>Dr. Mohamed F. AbuElyazeed</b>	(Thesis Advisor)
<b>Dr. Mohamed Yousef Abdallah</b>	(Internal Examiner)
<b>Dr. Sameh Assem Ibrahim</b>	(External Examiner)

Professor  
Faculty of Engineering, Ain Shams University

**Title of Thesis:**

**An Integrated Simultaneous Thermal and RF Energy Harvesting System  
for Wireless Sensor Networks**

**Key Words:**

Energy Harvesting; charge pump; maximum power point tracking; power combining; wireless sensor networks

**Summary:**

This work presents an integrated simultaneous thermal/RF energy harvesting system that is suitable for low power wireless sensor networks. The system has the ability to combine harvested energy from both DC and AC sources at the same time and provide a regulated output voltage of 1.75V feeding a current load from 0.15 mA to 0.77 mA. A triple mode maximum power point tracking (MPPT) algorithm is implemented to achieve the best possible efficiency at different source and load conditions. The three reconfigurable parameters in the system are the number of stages of the DC path, the frequency driving the charge pump, and the capacitors of the matching network in the RF-path. The energy harvester also enables the storage of extra power by charging a supercapacitor in order to use it during power shortage periods. The supercapacitor is charged using a voltage doubler that has an output of 3.5V. The system is implemented in a 180 nm CMOS technology and utilizes a total on-chip capacitance of 2.4 nF. Simulations show that the overall end-to-end efficiency of the system reaches a maximum of 60.5% at input thermal voltage of 350mV and RF input power of -8 dBmW.

# Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Ahmed Abdulraouf Awad Ahmed Helaly

Date:

Signature:

# Acknowledgements

I would like to express my sincere gratitude to my advisors, Dr. Ahmed Nader and Dr. Mohamed Fathy for their wise guidance and invaluable suggestions to this work. Their passion and dedicated involvement have inspired me a lot on both technical and personal levels.

I would also like to thank my family and friends for their endless support throughout the period of completing this work .

# Table of Contents

<b>Disclaimer</b>	<b>i</b>
<b>Acknowledgements</b>	<b>ii</b>
<b>Table of Contents</b>	<b>iii</b>
<b>List of Tables</b>	<b>vi</b>
<b>List of Figures</b>	<b>vii</b>
<b>List of Symbols and Abbreviations</b>	<b>xi</b>
<b>List of Publications</b>	<b>xiii</b>
<b>Abstract</b>	<b>xiv</b>
<b>1 INTRODUCTION</b>	<b>1</b>
1.1 Motivation . . . . .	1
1.1.1 Thermoelectric Generator . . . . .	1
1.1.2 RF Transducer . . . . .	3
1.1.3 Piezoelectric Transducer . . . . .	3
1.1.4 Photovoltaic Transducer . . . . .	4
1.2 Energy Harvesting Systems Characteristics . . . . .	5
1.3 Thesis Objective . . . . .	5
1.4 Thesis Outline . . . . .	6
<b>2 LITERATURE REVIEW</b>	<b>7</b>
2.1 Charge Pump Design . . . . .	7
2.1.1 Parallel-Series Charge Pump . . . . .	7
2.1.2 Fibonacci Charge Pump . . . . .	8
2.1.3 Dickson Charge Pump . . . . .	9
2.1.4 Pelliconi Charge Pump . . . . .	10
2.1.4.1 Pelliconi Charge Pump Theory of Operation . . . . .	11



2.1.4.2	Pelliconi Charge Pump Governing Equations . . . . .	12
2.1.4.3	Pelliconi Structure as a Rectifier . . . . .	14
2.2	Hybrid Energy Harvesting Systems . . . . .	18
2.2.1	Ultra Low Power On-Chip Hybrid Start-Up Energy Harvesting System . . . . .	19
2.2.2	Platform Architecture for Solar, Thermal, and Vibration Energy Combining With Single Inductor . . . . .	20
2.2.3	Simultaneous Multi-Source Integrated Energy Harvesting System for IoE Applications . . . . .	21
2.2.4	A Hybrid Energy Harvesting System With Rectifying-Combination and Improved Fractional-OCV MPPT Method . . . . .	22
2.3	Literature Review Conclusion . . . . .	23
<b>3</b>	<b>PROPOSED SYSTEM</b>	<b>24</b>
3.1	System Overview . . . . .	25
3.2	System Detailed Top Level Implementation . . . . .	26
3.2.1	MPPT FSM Algorithm . . . . .	27
3.2.1.1	Number of Charge Pump Stages . . . . .	27
3.2.1.2	DCO Frequency . . . . .	29
3.2.1.3	Matching Network Capacitance . . . . .	31
3.2.2	Output Regulation . . . . .	33
3.2.3	Storage Controller . . . . .	33
<b>4</b>	<b>CIRCUIT IMPLEMENTATION AND RESULTS</b>	<b>35</b>
4.1	Charge Pump Implementation . . . . .	35
4.1.1	Charge Pump Stage . . . . .	36
4.1.2	Inter-Stage Switches . . . . .	39
4.2	Output Sampling Circuit Implementation . . . . .	39
4.2.1	Output Sampling Circuit Comparator . . . . .	40
4.3	Rectifier and Matching Network Implementation . . . . .	45
4.4	DCO Implementation . . . . .	50
<b>5</b>	<b>SYSTEM INTEGRATION</b>	<b>56</b>
5.1	Integrated System Simulations . . . . .	57

5.1.1	Transient Analysis of the Integrated System . . . . .	57
5.1.2	MPPT FSM Performance Verification . . . . .	57
5.1.3	Output Regulation and Storage Controller . . . . .	61
5.1.4	End to End Efficiency of the Overall System . . . . .	62
5.2	System Layout . . . . .	64
5.2.1	Charge Pump Layout . . . . .	64
5.2.2	Output Sampling Circuit Layout . . . . .	65
5.2.3	DCO Layout . . . . .	65
5.2.4	Output Regulation Circuitry Layout . . . . .	65
5.2.5	Rectifier and Matching Network Layout . . . . .	68
5.2.6	Top Level Layout . . . . .	68
5.3	Comparison with the state-of-the-art projects . . . . .	68
<b>6</b>	<b>CONCLUSION AND FUTURE WORK</b>	<b>71</b>
6.1	Conclusion . . . . .	71
6.2	Future Work . . . . .	72
	<b>References</b>	<b>73</b>

# List of Tables

3.1	Output Regulation Logic Truth Table . . . . .	33
4.1	Charge Pump Bypass Logic Table . . . . .	36
4.2	Charge Pump ENABLE Logic Table . . . . .	36
4.3	Rectifier Simulation Results for Different Sizing . . . . .	46
4.4	Binary to Thermometer Coding for the 3 MSBs of the DCO . . . . .	52
5.1	Comparison with the-state-of-the-art Multi-Source Energy Harvesting Systems . . . . .	69

# List of Figures

1.1	Physical model for a Thermoelectric generator [8] . . . . .	2
1.2	Circuit model for a Thermoelectric generator . . . . .	2
1.3	Basic Block Diagram for RF Transducer . . . . .	3
1.4	Photovoltaic Cell Output Power vs Output Voltage for Different Illumina- tions [11] . . . . .	4
2.1	Parallel-Series Charge Pump Structure . . . . .	8
2.2	Fibonacci Charge Pump Structure . . . . .	9
2.3	Dickson Charge Pump Basic Structure . . . . .	9
2.4	Dickson Charge Pump MOS-Based Structure . . . . .	10
2.5	Pelliconi Charge Pump as a Boosting DC-DC Converter . . . . .	11
2.6	Pelliconi Charge Pump as a Boosting DC-DC Converter during $\phi_1$ . . . .	12
2.7	Pelliconi Charge Pump as a Boosting DC-DC Converter during $\phi_2$ . . . .	13
2.8	Coth Function Response . . . . .	14
2.9	Pelliconi Structure Operating as a Rectifier . . . . .	15
2.10	Pelliconi Rectifier with a Boost Converter Setup . . . . .	17
2.11	Waveforms of Rectifier Intermediate and Output Nodes . . . . .	17
2.12	RF Chain for Energy Harvesting . . . . .	18
2.13	Architecture of Hybrid Start-up Block Composed of Solar and RF Energy Harvesters . . . . .	19
2.14	Basic Diagram of Several Energy Sources Harvesting Utilizing a Single Inductor . . . . .	20
2.15	Block diagram of Simultaneous Multi-Source Integrated Energy Harvest- ing System . . . . .	21
2.16	Implementation of Boost Converter Using Reconfigurable Dickson Charge Pump . . . . .	21
2.17	Complete schematic of the Circuit Interface for the Thermal/RF Hybrid Harvesting . . . . .	22
3.1	Basic Block Diagram of the Proposed System . . . . .	26

3.2	Detailed implementation of the proposed system . . . . .	27
3.3	Vout Variation for Different N Values for Iout=0.5mA and Iout=0.4 mA . . . . .	29
3.4	Flow Chart Diagram for Number of Stages Optimization . . . . .	30
3.5	Rin Variation with switching frequency for N=4 and Vs= 0.8V . . . . .	31
3.6	Matching Network Implementation . . . . .	32
3.7	Output Voltage Regulation Loop . . . . .	34
3.8	Storage Controller Circuit Diagram . . . . .	34
4.1	Proposed Five Stage Pelliconi Charge Pump . . . . .	36
4.2	Efficiency of the Charge Pump under Different MOS Devices Sizing . . . . .	38
4.3	Bootstrapped Switch used for the implementation of inter-stage switches . . . . .	40
4.4	Output Sampling Circuit Implementation . . . . .	41
4.5	Output Sampling Comparator Implementation . . . . .	42
4.6	SR Latch Implementation . . . . .	42
4.7	Simulation Results of the Comparator with Input Test Signal between 800mV and 900mV . . . . .	43
4.8	Zoomed Version of the Simulation Results of the Comparator with Input Test Signal between 800mV and 900mV . . . . .	43
4.9	Post Layout Delay of the Comparator across Temperature for Extreme Corners . . . . .	44
4.10	Post Layout Current Consumption of the Comparator across Temperature for Extreme Corners . . . . .	44
4.11	Post Layout Monte Carlo Simulation Results for the Input Referred Offset of the Comparator . . . . .	45
4.12	Matching of the Rectifier with the Antenna Impedance on Smith Chart . . . . .	47
4.13	Transient Analysis of the Rectifier with the Matching Network. The red and blue signals are the input and output signals to the matching network respectively. The black signal is the output of the rectifier . . . . .	48
4.14	Zoomed Version of the Transient Analysis of the Rectifier with the Match- ing Network . . . . .	48
4.15	Matching of the Rectifier Impedance before Capacitance Adjustment when Rectifier Voltage is 1V . . . . .	49

4.16 Matching of the Rectifier Impedance after Capacitance Adjustment when Rectifier Voltage is 1V . . . . .	50
4.17 Matching of the Rectifier Impedance before Capacitance Adjustment when Rectifier Voltage is 1.2V . . . . .	51
4.18 Matching of the Rectifier Impedance after Capacitance Adjustment when Rectifier Voltage is 1.2V . . . . .	51
4.19 Current Steering DAC of the Implemented DCO . . . . .	53
4.20 Three Stage Current Starved DCO Implementation . . . . .	54
4.21 DCO Frequency against Different DCO Digital Words . . . . .	54
4.22 Total DCO Current Consumption (Analog and Digital parts) against Different DCO Digital Words . . . . .	54
4.23 MOSCAP Capacitance at Extreme Corners . . . . .	55
4.24 Non Overlapping Circuit to generate Charge Pump Clock Signals . . . . .	55
4.25 Simulation of the Non Overlapping Circuit at highest frequency . . . . .	55
5.1 Transient Simulation of the Overall System . . . . .	58
5.2 Simulation of the MPPT FSM performance for Adjusting Charge Pump Number of Stages . . . . .	58
5.3 Simulation of the MPPT FSM performance for adjusting Charge Pump Switching Frequency . . . . .	59
5.4 Charge Pump Input Voltage Variations during the Frequency Adjustment Process . . . . .	60
5.5 Simulation of the MPPT FSM performance for adjusting Matching Network Capacitors . . . . .	60
5.6 Output Voltage increases by about 25 mV upon Matching Network Capacitance Adjustment . . . . .	61
5.7 Simulation Results of the Output Regulation with the Storage Controller Enable . . . . .	61
5.8 Output Regulation with the Storage Controller Enable and VSC . . . . .	62
5.9 End-to-end efficiency of the proposed system against $V_{DC}$ at different $P_{RF}$ . . . . .	63
5.10 End-to-end efficiency of the proposed system against $P_{RF}$ at different $V_{DC}$ . . . . .	63
5.11 Charge Pump Layout . . . . .	64
5.12 Output Sampling Circuit Layout . . . . .	65

5.13 Strong Arm Comparator Layout . . . . .	66
5.14 Current Steering DAC Layout . . . . .	66
5.15 Digitally Controlled Oscillator Layout . . . . .	67
5.16 Regulation Circuitry Layout . . . . .	67
5.17 Rectifier and Matching Network Layout . . . . .	68
5.18 Top Level Layout . . . . .	70