بسم الله الرحمن الرحيم

MONA MAGHRABY

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

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MONA MAGHRABY

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Computer Engineering and Systems

Behavioral Modeling of Mixed-Signal Circuits

A Thesis submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Computer Engineering and Systems)

by

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Bachelor of Science in Electrical Engineering

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Degree: **Master of Science in Electrical Engineering (Computer and Systems Engineering)**

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Verifying the behavior of mixed-signal ICs is becoming more costly and complicated. ICs contain both analog and digital content with complex interactions between both domains, requiring simulation with both the analog and the digital content, to do so, co-simulation (mixed-signal simulation) is used, and this special type of simulation requires both analog and digital simulators.

Analog behavioral languages (e.g. Verilog-A) use a higher level of abstraction, to significantly reduce simulation time compared to full spice simulations. With the introduction of Verilog-AMS, came the ability to model mixed-signal circuits using both analog and digital behavioral languages (Verilog-A, Verilog), showing an advantage over analog behavioral language in terms of abstraction and speed, but still requiring an analog solver.

The simulation of the digital blocks in separation from the analog circuits can mask a lot of design issues. Mixed-signal simulators can simulate the netlist-based analog portion using an analog solver, and the digital portion using a digital simulator showing better correlation with a great simulation time reduction.

SystemVerilog supports real nets using nettype, which is a user-defined net that can be defined as a real net, it can be used to model analog circuits, this is an example of Real Number modeling.

In this work, we propose using SystemVerilog to accurately model the analog behavior of several blocks constituting a Phase Locked Loop using the nettype construct to create a composite

net, this is known as Real Number Modeling (RNM), and compare the results of simulating the real number model versus the analog transistor-level netlist.

Thesis Summary

With the widespread usage of SoC's containing mixed-signal circuits, verifying the behavior of top level mixed-signal ICs is becoming more costly and complicated. ICs contain both analog and digital content with several levels of interaction between both domains, these mixed-signal ICs need to be simulated with both the analog and the digital content, to do so, co-simulation or mixed-signal simulation is carried out, this special type of simulation requires an analog simulator to handle simulating the analog transistor-level circuits, and a digital event-based simulator to handle the digital HDL content, the mixed-signal simulator handles the synchronization and adapting the signals between the digital discrete time, logic-state based domain and the analog continuous time, continuous amplitude domain.

These simulations need to be carried out under a multitude of test scenarios to ensure the correct operation of the chip in different modes and under different inputs. These simulations can be very time consuming due to the presence of the analog solver that needs to solve huge circuit matrices, several techniques exist to model analog behavior using a higher abstraction (analog HDL languages).

Analog behavioral languages such as Verilog-A use a higher level of abstraction, offering a significant reduction in simulation time compared to full spice simulations [1], but it still requires an analog simulator, and doesn't readily fit into a digital verification framework.

With the introduction of Verilog-AMS, came the ability to model mixed-signal circuits, like PLLs [2], using both analog behavioral languages (Verilog-A) and digital event-driven HDL (Verilog), this can show an advantage over pure analog behavioral language in terms of abstraction and simulation speed, but still, an analog solver is required to simulate the continuous time Verilog-A section of the Verilog-AMS code.

At the same time, the simulation of the digital blocks in separation from the analog circuits can mask a lot of design issues. Mixed-signal simulators can simulate the netlist-based analog portion using an analog solver, and the event-based digital portion using a digital simulator showing a high level of correlation and accuracy with a great simulation time reduction.

SystemVerilog added the support of real nets using the new construct nettype [3], which is a user-defined net that can be defined as a real net, this real net can be used to model analog circuits [4].

In this work, we propose using a digital HDL language (SystemVerilog) to accurately model the analog behavior of several blocks constituting a Phase Locked Loop using the nettype construct to create a composite net, this is known as Real Number Modeling (RNM), and compare the results of simulating the real number model versus the analog transistor-level netlist.

Key words:

RNM, Real Number Modeling, Behavioral Modeling, SystemVerilog, z-transform, PLL, Phase-locked Loops, Lookup Table, nettypes