بسم اللّه الرحمن الرحيم

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بالرسالة صفحات
لم ترد بالأصل

Ain Shams University
Faculty of Engineering
Electronics and Electrical Communications
Engineering Department

Injection Locked Oscillators

**A Thesis submitted in partial fulfillment for the requirements of
a Master of Science degree in Electrical Engineering
Electronics and Electrical Communications Engineering Department**

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B.Sc. of Electrical Engineering
(Electronics and Electrical Communications Engineering Department)
Ain Shams University, 2016

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Cairo 2020

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Statement

This Thesis submitted in partial fulfillment for the requirements of a Master of Science degree in Electrical Engineering, Electronics and Electrical Communications Engineering Department.

The work included in this thesis was carried out by the author at the Electronics and Electrical Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

Khaled Mohamed Elsayed Salem "Injection Locked Oscillators", Master of Science dissertation, Ain Shams University, 2020.

Clock and frequency synthesizers are essential block in any wireless or wireline transceivers also they play a critical role in the performance of any microprocessor. The frequency synthesizers should meet the stringent requirements imposed by the modern systems in terms of low jitter, low power and small area. Conventionally, the frequency synthesizers and clock multipliers are realized using phase locked loops (PLLs). However, the low jitter requirement is difficult to achieve in PLLs without high power consumption and large area. New architectures and techniques are investigated in literature to overcome this tradeoff.

This thesis aims to investigate and design a low-jitter clock multiplier using injection locking which is a promising technique that can overcome the tradeoffs in the other conventional clock multipliers. A ring-based injection-locked oscillator with continuous frequency-tracking loop (FTL) is proposed that generates an output clock from 2.4 GHz to 2.8 GHz. The FTL maintains the oscillator inside its lock range across process, supply and temperature (PVT) variations. A reference frequency quadrupler is proposed with a duty cycle correction circuit that lowers the deterministic jitter of its output clock. A high multiplication factor of 56 is achieved using the frequency quadrupler with the injection locked clock multiplier. Finally, the proposed design is implemented using 130-nm CMOS process and achieves a high figure-of-merit (FoM) compared to the state of art designs.

Keywords: Injection-locked ring oscillator, Injection-locked clock multipliers, Frequency tracking loop, Reference frequency quadrupler, Duty cycle correction, Phase-locked loops.

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Summary

This thesis is divided into five chapters as follows:

Chapter 1 gives an introduction to the frequency synthesizers and clock multipliers applications such as wireless and wireline transceivers. Then it presents the performance challenges which face the conventional frequency synthesizers. Finally, it shows the motivation of this thesis followed by the thesis organization.

Chapter 2 provides a literature survey for high-performance clock multipliers such as multiplying delay-locked loops and injection-locked oscillators. Then a detailed survey for injection-locked oscillators and their frequency calibrators is presented.

Chapter 3 shows the system design and the noise analysis for the proposed injection-locked clock multiplier. Then it discusses the design of injection-locked oscillator and its predicted locking range. Finally, the design of the frequency-tracking loop and its building blocks are demonstrated in details followed by the simulation results and performance comparison with the state of art designs.

Chapter 4 depicts the proposed reference frequency quadrupler with duty cycle correction loop to be integrated with the injection-locked clock multiplier. Then the achieved results are compared with the state of art frequency quadruplers.

Chapter 5 concludes and summarizes the work presented in this thesis as well as proposes suggestions for the future work to further optimize the performance.