شبكة المعلومات الجامعية

بسم اللّه الرحمن الرحيم

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

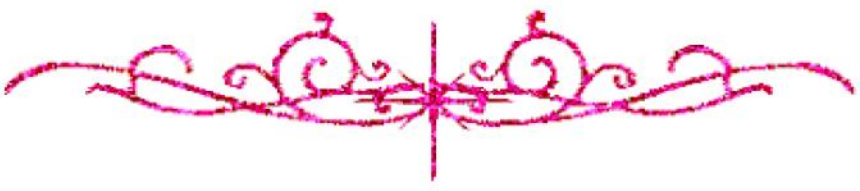
نقسم باللّه العظيم أن المادة التي تم توثيقها وتسجيلها علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار

شبكة المعلومات الجامعية

بعض الوثائق الأصلية تالفة



بالرسالة صفحات
لم ترد بالأصل

LOW-NOISE WIDE-BANDWIDTH PHASE-DOMAIN ALL-DIGITAL FRACTIONAL-N PHASE-LOCKED LOOP

By

Kareem Ramadan Mahmoud Rashed

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING ,CAIRO UNIVERSITY
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Title of Thesis:

Low-Noise Wide-Bandwidth Phase-Domain All-Digital Fractional-N Phase-Locked Loop

Key Words:
All-Digital Phase-Locked Loop (ADPLL); Low Power; Wide Bandwidth; Time-to-Digital Converter (TDC); Digital-to-Time Converter (DTC)

Summary:
In this thesis, an ADPLL that employs a high-resolution TDC and a high-linearity DTC to achieve low in-band phase noise and spurs with wide bandwidth and low power consumption is presented. The TDC/DTC set is implemented in TSMC-40nm CMOS process. A time-amplifier based TDC (TA-TDC) is utilized to achieve a sub-gate delay resolution of 3.2 pS. The TA-TDC achieves an integral nonlinearity (INL) less than 0.5 LSB and power consumption of 108 uW. A constant-slope DTC (CS-DTC) that leverages the concept of charge redistribution is proposed. The CS-DTC achieves 0.3 LSB INL. Consequently, a fractional spur of level better than -48 dBc/Hz is expected at the PLL output. The DTC achieves 1.7 pS_{rms} integrated jitter which dominates the in-band phase noise of the PLL. The CS-DTC consumes only 8 uA from 1.1 V supply. The PLL was able to achieve 1.44 MHz bandwidth at 2.5 GHz output frequency using 50 MHz reference. The PLL achieves better than -106 dBc/Hz in-band phase noise which translates to an integrated RMS-jitter of 682 fS.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

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