



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكرو فيلم

بسم الله الرحمن الرحيم



HANAA ALY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم



شبكة المعلومات الجامعية التوثيق الإلكتروني والميكروفيلم



HANAA ALY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

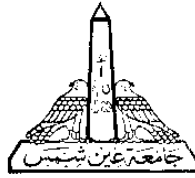


يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار



HANAA ALY



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Electro-Thermo-Mechanical Modeling of Relaxed-Stress TSVs

A Thesis submitted in partial fulfillment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

(Electronics Engineering and Electrical Communications)

By

Amira Nabil Ali Ali

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2013

Supervised By

Prof. Dr / Hani Ferky Mohammed Ragai

Electronics and Communications ,

Ain Shams University

Prof. Dr / Christian Gontrand

Electronics and Communications ,

INSA-loyn University

Dr / Mohammed Abd-Elhamid Abouelatta

Electronics and Communications ,

Ain Shams University

Dr / Ahmed Shaker Ghazala

Physics and Mathematics ,

Ain Shams University

Cairo - (2021)



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications

Electro-Thermo-Mechanical Modeling of Relaxed-Stress TSVs

By

Amira Nabil Ali Ali

Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2013

Examiners' Committee

Name and Affiliation

Signature

Prof. Dr / Hanady Hussien Issa

.....

Electronics and Communications , Arab Academy for science,
Technology and Maritime Transport.

Prof. Dr / Abd El-Halim Abd El-Nabi Zekry

.....

Electronics and Communications , Ain Shams University

Prof. Dr / Hani Fekry Mohammed Ragai

.....

Electronics and Communications , Ain Shams University.

Dr / Mohammed Abd-Elhamid Abouelatta

.....

Electronics and Communications , Ain Shams University

Date: 18 March 2021

Statement

This thesis is submitted as a partial fulfillment of Doctor of Philosophy in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Amira Nabil Ali

Signature

.....

Date:

Researcher Data

Name	: Amira Nabil Ali
Date of birth	: 6 / 4 / 1984
Place of birth	: Cairo, Egypt.
Last academic degree	: Master of Science.
Field of specialization	: Electronic and Communication Engineering.
University issued the degree	: Ain Shams University.
Date of issued degree	: 2013
Current job	: Assistant Lecturer.

Thesis Summary

3D integration has emerged as an effective way to improve the performance of microelectronic devices. Compared with 2D classical schemes, 3D integration has a lot of benefits such as shorter interconnection, heterogeneous integration, and power consumption reduction. In this regard, Through Silicon Vias (TSVs) provide the vertical connection between stacked chips. They minimize the interconnect paths leading to a reduction in parasitic capacitance and resistance and offer small packaging sizes. However, TSV interconnects face some challenges in design and fabrication. Some of these issues are via etching and filling, thermal management, and floor planning.

Due to differences in the coefficient of thermal expansion (CTE) between the bulk and the TSV filling material, stresses are generated in the bulk around the TSV during thermal cycles. These generated stresses may lead to damage or crack of the wafer and interfacial delamination of TSV. Moreover, the mobility of carriers is changed due to the generated stresses. There would be an area around TSV where the transistors and active elements should be put away. This area is called keep out zone (KOZ) where the stresses are very high and affect the reliability of transistor performance.

Tunnel field effect transistor (TFET) is proposed as a good alternative to MOSFET transistors where the current is mainly due to band to band tunneling phenomena instead of thermionic emission as in traditional MOSFETs. TFET has advantages over MOSFET of low leakage current, low power supply, and a better I_{ON}/I_{OFF} ratio. However, some challenges face the

design of TFET. The ambipolarity and high threshold voltage V_{th} are the main concern in TFET structures.

In this thesis, a complete study of TSV is presented under different conditions to figure out the best conditions for reliability. The TSV generated stress is analyzed using thermo-mechanical modeling to calibrate the thermal parameters of the materials used. Then a Finite element analysis using Sentaurus TCAD tool is utilized to study TSV's generated stresses at different conditions including different annealing temperatures, different via diameters, and different liner thicknesses. Then, a KOZ determination is done to find a relation between annealing temperature, via's radius, and KOZ area. Also, Carbon Nanotubes (CNTs) are used as a filling material instead of Copper to further reduce the generated stresses and decrease the KOZ. A Cu/CNT composite is analyzed also and a ratio of CNT to Cu is presented.

Next, a comprehensive study of TFET is provided as an alternative of MOSFETs including different structures of TFET, non-silicon source TFET, all non-silicon TFET, and a hybrid dielectric gate oxide TFET. Then, a further enhancement to TFET is provided for low power applications. This study is used next to compare bulk MOSFET with bulk TFET under via's stresses.

Finally, a study of the generated stress's effects on transistors is presented and analyzed. The influence on the currents and carrier mobility of both TFET and MOSFET are compared for the same channel orientation and same distance.

Acknowledgment

I would like to thank my supervisors, Prof. Hani Fekri, Prof. Gontrand, Dr. Mohammed Abouelatta, and Dr. Ahmed Shaker for giving me the opportunity to be one of their students and guiding me through my work. Without your support and clear guidance, my work would not have been done. Thank you very much for all your help and guidance.

To my father's soul, it was your dream. I am sure you will feel it. May God bless your soul.

To my mother and all my family, you deserve all the credit for this accomplishment, as you have supported me every step of the way with complete selflessness. Thank you for your unconditional love.

A great thanks to Eng. Mai Adel for your collaboration and friendship.

To Dr. Enas Elgabbas, thank you for all your help and support.

Also, I would like Eng. Ahmed Fathy for his help and I very much appreciate the collaboration and friendship from all my mates.

Last, I am deeply thankful to Eng. Mahmoud Sadat for his help with my tool.

March 2021

Table of Contents

THESIS SUMMARY	I
ACKNOWLEDGMENT	IV
TABLE OF CONTENTS	V
LIST OF FIGURES	VII
LIST OF TABLES	XII
LIST OF SYMBOLS	XIII
LIST OF ABBREVIATIONS	XV
CHAPTER 1: INTRODUCTION	1
1.1 Introduction	2
1.2 Literature Review	4
1.3 Thesis Contribution	10
1.4 Sentaurus TCAD Simulation Tool	10
1.5 Thesis Organization	11
CHAPTER 2: TSV'S THERMO-MECHANICAL ANALYSIS	13
2.1 Introduction	14
2.2 Analytical analysis of through silicon via	15
2.3 TSV geometry	20
2.4 Simulation analysis of through silicon via	22
2.4.1 Different annealing temperature	23
2.4.2 Different via radii	25
2.4.3 Different Liner thickness	27
2.5 Keep out Zone Determination	29
2.5.1 KOZ at different annealing temperatures	30
2.5.2 KOZ at different via radii	32
2.6 Carbon Nanotubes	34
2.6.1 Analytical analysis of CNT-filled TSV	36
2.6.2 Analysis of Cu/CNT-filled TSV	38
2.7 TSV Trading off	41
2.8 Summery	42
CHAPTER 3: TSV INDUCED STRESS EFFECTS ON MODERN 3D INTEGRATION DEVICES	43
3.1 Introduction	44
3.2 Tunnel FET operation principles	45
3.3 Modeling of Band to band tunneling (BTBT)	47
3.4 Simulation and Calibration of TFET	48

3.4.1 Different Silicon TFET structures	49
3.4.2 Non-Silicon source material TFET	51
3.4.3 Non-Silicon TFET	53
3.4.4 Hybrid-dielectric gate oxide TFET	54
3.4.6 Comparison of TFET types	54
3.5 Low power TFET	56
3.5.1 All Silicon Structure	56
3.5.2 All InAs Structure	57
3.6 Hetero-dielectric Ge-source TFET enhancement study	62
3.7 TSV Induced Stress Effects	66
3.7.1 Simulation Structure Setup	68
• NMOS process flow	68
• TFET process flow	69
3.7.2 Simulation Results	70
• TSV effects on MOS	70
• TSV effects on TFET	71
3.8 Summery	74
CHAPTER 4: CONCLUSION AND FUTURE WORK	75
4.1 Conclusion	76
4.2 Future Work	77
REFERENCES	79

List of Figures

Figure 1.1: Cu Protrusion [18] at (a) Different via radii (b) Different TSV length (c) TSV pitches (d) Different annealing temperature	6
Figure 1.2: Average Cu protrusion at different annealing temperature [19].	6
Figure 1.3: (a) Structure of TTSV (b) Stress with/without CNT as a core material [30]	8
Figure 2.1: TSV process flow schemes.	13
Figure 2.2: TSV structure used in the analytical analysis	15
Figure 2.3: Analytical radial stress with and without barrier effect.	16
Figure 2.4: TSV structure used to calibrate TCAD tool (a) Cross section area (b) 3D Geometry of TSV.	17
Figure 2.5: Comparison between analytical and simulation results (a) analytical results without correction factor (b) analytical results with the correction factor.	18
Figure 2.6: Through Silicon via profiles (a) taper (b) straight. (c) re-entrant	19
Figure 2.7: Simulation results of different TSV profiles.	21
Figure 2.8: Simulated stress profile at different T_{ann} (a) 250 °C (b) 350 °C (c) 400 °C (d) 450 °C	23
Figure 2.9: The radial stresses at different annealing temperatures.	23
Figure 2.10: Average protrusion at different annealing temperatures.	24
Figure 2.11: Simulated stress profile at different via radius (a) 1 μm (b) 1.5 μm (c) 2 μm (d) 3 μm	25
Figure 2.12: The radial stresses at different via radii.	25

Figure 2.13 Average protrusion at different via radii.	26
Figure 2.14: Simulated stress profile at different oxide liner thickness (a) 0.2 μ m (b) 0.3 μ m	27
Figure 2.15: The radial stresses at different oxide liner thickness.	27
Figure 2.16 Average protrusion at different oxide liner thickness.	27
Figure 2.17 Mobility change (a) (100) orientation when $T_{ann} = 250$ $^{\circ}$ C (b) (110) orientation when $T_{ann} = 250$ $^{\circ}$ C (c) (100) orientation when $T_{ann} = 350$ $^{\circ}$ C (d) (110) orientation when $T_{ann} = 350$ $^{\circ}$ C (e) (100) orientation when $T_{ann} = 400$ $^{\circ}$ C (f) (110) orientation when $T_{ann} = 400$ $^{\circ}$ C (g) (100) orientation when $T_{ann} = 450$ $^{\circ}$ C (h) (110) orientation when $T_{ann} = 450$ $^{\circ}$ C	30
Figure 2.18 Mobility change (a) (100) orientation when radius = 1 μ m (b) (110) orientation when radius = 1 μ m (c) (100) orientation when radius = 1.5 μ m (d) (110) orientation when radius = 1.5 μ m (e) (100) orientation when radius = 2 μ m (f) (110) orientation when radius = 2 μ m (g) (100) orientation when radius = 3 μ m (h) (110) orientation when radius = 3 μ m	32
Figure 2.19: Different between SWCNT and MWCNT.	34
Figure 2.20: SWCNT's different structures.	34
Figure 2.21: Bottom-up approach of CNT synthesis	35
Figure 2.22: CNT synthesis using additional wafer	35
Figure 2.23: CTE for CNT.	37
Figure 2.24: Simulation and analytical results for CNT at (a) $T_{ann} = 400$ $^{\circ}$ C. (b) $T_{ann} = 500$ $^{\circ}$ C	37
Figure 2.25: Simulation results of partially filled annular Cu-TSV.	38
Figure 2.26 Mobility change (a) (100) orientation when CNT is 25%	39