



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكرو فيلم

بسم الله الرحمن الرحيم



HANAA ALY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم



شبكة المعلومات الجامعية التوثيق الإلكتروني والميكروفيلم



HANAA ALY



شبكة المعلومات الجامعية
التوثيق الإلكتروني والميكروفيلم

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات



يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار



HANAA ALY



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Digital Testing of Analogue Circuits

A Thesis submitted in partial fulfilment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Bassam Abdelwahab Aboelftooh

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, MTC, 2012

Supervised By

Prof. Hani Fikry Ragaay

Assoc. Prof. Mohammed Hassan Elmahlawy

Assoc. Prof. Sameh Aasem Ibrahim

Cairo - (2021)



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications

Digital Testing of Analogue Circuits

by

Bassam Abdelwahab Aboelftooh

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, MIU, 2020

Examiners' Committee

Name and Affiliation

Signature

Prof. El-Sayed Mostafa Saad

.....

Electronics and Communications , Helwan University

Prof. Mohamed Amin Ebrahim Dessouky

.....

Electronics and Communications , Ain Shams University

Prof. Hani Fikry Ragaay

.....

Electronics and Communications , Ain Shams University

Assoc. Prof. Mohamed Hassan Elmahalawy

.....

Electronics and Communications , Future University

Statement

This thesis is submitted as a partial fulfilment of Doctor of Philosophy in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Eng. Bassam Abdelwahab Aboelftooh

Signature

.....

Researcher Data

Name	: Bassam Abdelwahab Aboelftooh
Date of birth	: October 8,1982
Place of birth	: Cairo
Last academic degree	: Master of Science in Electrical Engineering
Field of specialization	: Biomedical Engineering
University issued the degree	: Military Technical College
Date of issued degree	: October, 2012
Current job	: Lecturer Assistant

Thesis Summary

This thesis presents the new parametric fault detection (PFD) approach for analog circuits testing. It combines different approaches to enhance the PFD, based on the proper selection of classified frequency-bands with different amplitude weights for fault controllability and the proper selection of test-points for fault observability. The analog test generator (ATG) that stimulates parametric faults in the analog circuit under test (ACUT) generates a test waveform that sweeps on an applicable frequency-band with amplitude weights instead of sweeping the whole frequency-band. The test response is compacted on each applicable frequency-band for digital signature generation. The summation of unwanted samples from other unwanted frequency-bands are avoided for efficient PFD, based on the digital signature curve (DSC) that plots the digital signatures versus each component variation. In addition, the hybrid between the advantage of the MATLAB and the PSPICE simulation is exploited to developed better worst-case analysis (WCA). The presented simulation results, applied to different analog benchmark circuits, show the significant improvement in the PFD compared to other previously published works, in terms of the classified frequency-band and the required number of test-points. In addition, it is found that the best selection of a test waveform is the sweeping-frequency of a sinusoidal waveform with different amplitude weights.

Key words:

Digital testing of analog circuits; testing of analog circuits; classification of frequency-bands; fault detection for parametric faults; selection of test-points.

Acknowledgment

I would like to thank the following people, without whom I would not have been able to complete this thesis, and without whom I would not have made it through my PhD degree

My supervisor Dr. M. H. Elmahlawy for his enthusiasm during the thesis, consistent support, encouragement and patience. I am extremely grateful for our friendly frequent meetings. And Prof. H. F. Ragaai, for his guidance, thoughtful comments and recommendations.

And my biggest thanks to my family for all the support you have shown me through this research; for my mother, who has the all the credit for all the best in my life and for always praying for me. For my wife for all her support and being responsible for our kids and being alone for long times while I am working on my thesis. For my kids, sorry for being even grumpier and busy than normal whilst I wrote this thesis.

July 2021

Contents

List of Figures	IV
List of Tables	VII
List of Abbreviations	VIII
Abstract	X
Chapter 1 Introduction	1
1.1 Motivation in the testing of analog circuits	1
1.2 Related works	4
1.3 Challenges in analog circuit testing	6
1.4 Thesis objectives and contributions	8
1.5 Thesis Organization	9
1.6 List of Publications	11
Chapter 2 Fault Diagnosis of Analog Circuits	12
2.1 Introduction	12
2.2 Fault classification	16
2.2.1 Manufacturing tolerances	16
2.2.2 Soft faults	16
2.2.3 Hard faults	16
2.2.4 Fatal faults	17
2.3 Fault detection objectives	18
2.3.1 Fault Detection	18
2.3.2 Fault Isolation	18
2.3.3 Fault Identification	18
2.3.4 Fault prediction	18
2.3.5 Fault Explanation	18
2.3.6 Fault Simulation	18
2.4 Electronic circuit testing	19
2.4.1 Design verification phase	19
2.4.2 Realization phase	20

2.4.3	Production phase	20
2.4.4	Field testing.....	21
2.5	Fault diagnosis techniques.....	22
2.5.1	SBT Techniques: Fault dictionary – Traditional methods	24
2.5.2	SBT Techniques: Fault dictionary – Intelligence methods.....	29
2.5.3	SBT Techniques: Statistical techniques	32
2.5.4	SAT techniques	32
2.6	Recent Researches Analysis.....	35
2.6.1	Number of Faults	35
2.6.2	Fault types	35
2.6.3	The benchmark ACUTs	36
2.6.4	Components Considered	36
2.6.5	Reputation of Simulation Tools	36
2.6.6	Timeline analysis	37
Chapter 3	Digital testing of analog circuit system.....	39
3.1	Introduction	39
3.2	Design Approach of the DTAC.....	43
3.1.1	Analog test pattern generator	44
3.1.2	Analog circuit under test	50
3.1.3	Digital compactor of the Analog Test response.....	53
3.3	PSPICE circuit simulation and MATLAB simulation	54
3.1.4	Worst-case Analysis of the ACUT.....	55
3.1.5	Signature Boundary Difference	62
3.4	Digital signature curve for analog circuits	63
3.5	Fault detection using the DSC.....	80
3.6	Conclusion.....	82
Chapter 4	Enhancement techniques for parametric fault detection	84
4.1	Introduction	84
4.2	Classified Frequency bands.....	85
4.3	Test-Point Selection	88

4.4	Amplitude Weights of Sinusoidal Test Waveforms.....	92
4.5	Non-Sinusoidal Test Waveforms and single-frequency test waveforms	100
4.6	ACUT Case Studies.....	108
4.6.1	Case Study I	108
4.6.2	Case Study II.....	110
4.6.3	Case Study III.....	112
4.6.4	Case Study IV	116
4.7	Comparison between the presented work and the other previously published works..	124
4.8	Conclusion.....	129
Chapter 5	Conclusion & Future Work.....	131
5.1	Conclusion.....	131
5.2	Future Work	132
References		134

List of Figures

Figure 2-1 Classification of analogue circuit faults [11].	13
Figure 2-2 Production cycle phases [11].	19
Figure 2-3 The Mean Time Between Failures (MTBF) [11].	21
Figure 2-4 Classification of fault diagnosis methods.	23
Figure 2-5 The block diagram of the Model-based fault diagnosis.	25
Figure 2-6 The block diagram of the Hierarchical based fault diagnosis.	25
Figure 2-7 The block diagram of the formula based fault diagnosis approaches.	26
Figure 2-8 The block diagram of Signal analysis based fault diagnosis.	26
Figure 2-9 The block diagram of the sensitivity analysis based technique	27
Figure 2-10 The block diagram of Measurement-based fault diagnosis.	27
Figure 2-11 The block diagram of the oscillation based technique	28
Figure 2-12 The block diagram of transform based fault diagnosis	29
Figure 2-13 The block diagram of the optimization-based method.	30
Figure 2-14 The block diagram of the rule-based process.	31
Figure 2-15 Block diagram of Machine learning based fault diagnosis	31
Figure 2-16 Block diagram of Hybrid approach based fault diagnosis	32
Figure 2-17 Analysis based on type of faults.	35
Figure 2-18 Analysis based on simulation tools used.	37
Figure 2-19 Time analysis.	38
Figure 3-1 Main flowchart of the presented analog testing approach.	43
Figure 3-2. Main block diagram of the presented analog testing approach.	44
Figure 3-3 Different standard test waveforms generated by the ATG.	45
Figure 3-4 Schematic diagram of the ATG using the PSPICE simulation for generating standard test waveforms.	47
Figure 3-5 Frequency sweep.	47
Figure 3-6 Timing diagram of the input sinusoidal test waveforms (green) and their FFT for (a) IW, (b) DW, (c) MW, (d) (CW), and their test response (Red) generated from the circuit with LPF characteristics.	49
Figure 3-7 Schematic diagram of the UAF used as the ACUT	50
Figure 3-8 the analysis of the ACUT using Filter Design Tool	52
Figure 3-9 Schematic diagram of the DCATR stage.	54
Figure 3-10 Timing diagram of the closing test window of the accumulation process for digital signature generation according to case study I, discussed in section V.	54
Figure 3-11 Worst-case transfer function (Max) using a) PSPICE simulation. b) MATLAB simulation.	57
Figure 3-12 Worst-case transfer function (Min) using a) PSPICE simulation. b) MATLAB simulation.	59

Figure 3-13 SBD of TP_{LPF} using different test waveforms with different amplitude weights using the Hybrid simulation.....	63
Figure 3-14 The amplitude response Vs. R_1 variations for using the PSPICE simulation	66
Figure 3-15 The pass-band gain and the bandwidth Vs. R_1 variations for using the PSPICE simulation	67
Figure 3-16 The DSC and DSB of R_1 using the Hybrid simulation	68
Figure 3-17 The DSC and DSB of R_1 using the MATLAB simulation.....	68
Figure 3-18 The amplitude response Vs. R_q variations for using the PSPICE simulation	69
Figure 3-19 The pass-band gain and the bandwidth Vs. R_q variations for using the PSPICE simulation	70
Figure 3-20 The DSC and DSB of R_q using the Hybrid simulation	71
Figure 3-21 The DSC and DSB of R_q using the MATLAB simulation.....	71
Figure 3-22 The amplitude response Vs. C_2 variations for using the PSPICE simulation	72
Figure 3-23 The pass-band gain and the bandwidth Vs. C_2 variations for using the PSPICE simulation	73
Figure 3-24 The DSC and DSB of C_2 using the Hybrid simulation	73
Figure 3-25 The DSC and DSB of C_2 using the MATLAB simulation.....	74
Figure 3-26 The amplitude response Vs. R_2 variations for using the PSPICE simulation	75
Figure 3-27 The pass-band gain and the bandwidth Vs. R_2 variations for using the PSPICE simulation	76
Figure 3-28 The DSC and DSB of R_2 using the Hybrid simulation	76
Figure 3-29 The DSC and DSB of R_2 using the MATLAB simulation.....	77
Figure 3-30 The amplitude response Vs. R_4 variations for using the PSPICE simulation	78
Figure 3-31 The pass-band gain and the bandwidth Vs. R_4 variations for using the PSPICE simulation	79
Figure 3-32 The DSC and DSB of R_4 using the Hybrid simulation	79
Figure 3-33 The DSC and DSB of R_4 using the MATLAB simulation.....	80
Figure 3-34 Undetectable parametric faults.	81
Figure 4-1 Amplitude responses of the three test-points	85
Figure 4-2 Classified frequency-bands of the TP_{LPF}	86
Figure 4-3 Classified frequency-bands of the TP_{HPF}	86
Figure 4-4 Classified frequency-bands of the TP_{BPF}	87
Figure 4-5 Schematic diagram and the amplitude response of the SKLPF.	111

Figure 4-6 Schematic diagram and the frequency-band classification of the BF.	114
Figure 4-7 schematic daigram, amplitude response of the ACUT with 11-TP	120
Figure 4-8 Schematic diagram of the Sallen-Key band-pass-filter.....	126