شبكة المعلومات الجامعية

بسم اللّه الرحمن الرحيم

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم باللّه العظيم أن المادة التي تم توثيقها وتسجيلها علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

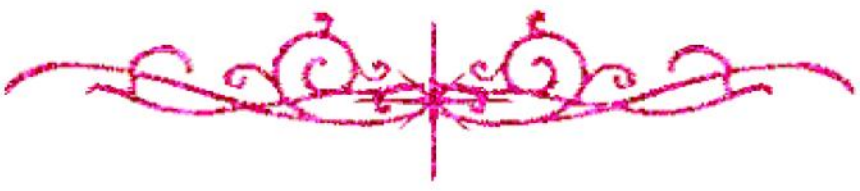
يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار

بالرسالة صفحات
لم ترد بالأصل

شبكة المعلومات الجامعية

بعض الوثائق الأصلية تالفة



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics and Communications Engineering Department

Computer Aided Design Of Gate Turn Off Thyristor

A Thesis

Submitted in Partial Fulfillment for the Requirements
of the Degree of Ph.D of Science in Electrical Engineering
(Electronics and Communications Engineering)

Submitted By

MOHAMMED ABD ELRAHMAN ABU-ELKAMAL

M.Sc. of Electrical Engineering
(Electronics and Communications Engineering)
Ain Shams University, 1999

Supervised By

Prof. Dr. ABDEL HALIM ZEKRY
Prof. Dr. MOHAMMAD ELSABA

Cairo - 2007

STATEMENT

This dissertation is submitted to Ain Shams University for the degree of P.h.D of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or qualification at any university or institution.

Date : / / 2006
Signature :
Name : Mohamed Abd El-Rahman Abu El-Kamal

ACKNOWLEDGMENT
All gratitude to ALLAH

I would like to express my sincere appreciation and deepest gratitude to prof. Dr. Abd El Halim Zekry for his continuous support and valuable guidance which he did with patience, care, and encouragement. I do not know how to thank prof. zekry.He was always there whenever I need him to answer my questions. I will always remember the precious discussions we had together. I feel very lucky to have been able to work with him over the past five years.

My sincere thanks to prof . Mohammad Elsabba for his continuous advice and recommendations during my research work.

I am also grateful to all professors, staff members, of electronics and communications engineering department, Ain Shams University who supported and encouraged me during my research. Also the staff of N.T.C.

Last but not least, my family who gave me moral support and encouragement to pursue my goals more than they realize. I cannot express the love and gratitude I feel for them.

Approval Sheet

Name : Mohamed Abd Elrahman Abu-Elkamal

Thesis : Computer aided design of Gate turn of Thyristor

Degree : Ph. D of Science in Electrical Engineering

	Name,Title and Affiliation	Signature
1.	Prof Dr. Elsayed Mostafa Saad Electronics and Communications Engineering Dept. Faculty of Engineering, Helewan University	
2.	Proof. Dr. Adel Ezzat Elhenawi Electronics and Communications Engineering Dept. Faculty of Engineering, Ain shams University	
3.	Proof . Dr. Abdel Halim Zekry Electronics and Communications Engineering Dept. Faculty of Engineering, Ain shams University	
4.	Proof. Dr. Mohammad El saba Electronics and Communications Engineering Dept. Faculty of Engineering, Ain shams University	

Date / 2007

Abstract

Eng. Mohammed AbuElkamal (Ph.D) computer aided design of power semiconductor devices- Egyptians Electricity Authority.

Recent progressing efforts in industrial electronics demands developing CAD models for both manufacturers and system designers. GTO is a very important power devices used in many fields of applications due to its nature the simulation of the device depend on physical models and needs a special software to solve mathematical equations describing the behavior of the device 2-D model. The main disadvantages of these software are there limited source codes and difficult languages. In this thesis we develop 2-D macro model using the general and famous CAD tools like SPICE. With a precise technique of parameter extraction our model gives accurate results in both static and dynamic behavior at low and high frequency up to 110 kHZ. Also we present the usual 1-D model. With these precise parameters the 1-D model provides very efficient results from DC up to 70 kHZ .This thesis fill the gap between the physical models and macro models.

Key word: GTO – Parameters extraction – 1-D,2-D models – Simulation results - SPICE

Abstract

Eng. Mohammed AbuElkamal (Ph.D) computer aided design of power semiconductor devices- Egyptians Electricity Authority.

Recent progressing efforts in industrial electronics demands developing CAD models for both manufacturers and system designers. GTO is a very important power devices used in many fields of applications due to its nature the simulation of the device depend on physical models and needs a special software to solve mathematical equations describing the behavior of the device 2-D model. The main disadvantages of these software are there limited source codes and difficult languages. In this thesis we develop 2-D macro model using the general and famous CAD tools like SPICE. With a precise technique of parameter extraction our model gives accurate results in both static and dynamic behavior at low and high frequency up to 110 kHZ. Also we present the usual 1-D model. With these precise parameters the 1-D model provides very efficient results from DC up to 70 kHZ .This thesis fill the gap between the physical models and macro models.

Key word: GTO – Parameters extraction – 1-D,2-D models – Simulation results - SPICE

Contents

*****

Chapter -1-
Introduction

Now, there are intensive research efforts in the computer-aided design of power electronic circuits because of the advent of the smart power IC's with large complexity. CAD tools are required to simulate and predict the performance of such complicated circuits before sending design to the silicon foundry.

The CAD tools of power electronic circuits lag behind the CAD tools for the conventional integrated circuits partly because of the complicated structure of power devices. To automate the analysis of the power electronic circuits in general and the smart power IC's in specific, one has to develop efficient device simulator. The development of such device simulator helps also to optimize the devices themselves for specific applications [1].

Several gate turn off thyristors GTO models have been developed for use in circuit simulators .In 1993, Yon-Tack chung et el [2] developed a GTO micro model for circuit simulation. This model based on the Ebers-Moll equations extended to include the three-junction devices. In 1994, K.J Tseng and P.R. Palmer [2] developed a GTO model for circuit simulation. This model uses analytical expressions to describe the internal physics. A comparison of measured and simulated waveforms was included. However, the methodology for the parameters extraction was not included.

In 1995, C.L. Ma et al [3] have developed a physics-based model for the GTO thyristors. Excellent agreement was found between simulated and

measured anode current and voltage waveforms. In 1995, M. Bayer et al [4] developed an analytical model of a GTO based on the calculation of the charge carrier distribution in the base layers by an approximation of the time derivatives. Effects like avalanche breakdown, recombination, back injection into the high-doped emitter and conductivity modulation are included.

Many power semiconductor device models were developed at the University of Washington through a research program supported by NSF-CDADIC (NSF Center for Design of Analog-Digital Integrated Circuits) during the period from 1990 through 1998. MSEE and ph.D. Students under the direction of professor peter O. Lauritzen developed most of the models [5]. Almost all of these models are now in the public domain, and they are available for public downloading of model source code and documentation. Several newer and updated models have been added from other universities.

Three of the models were developed with partial support from Siemens AG (now Infineon) [5] and one with partial support from EPRI (Electric power Research Institute) [5]. Students at the Indian Institute of Technology , Madras, India also developed some models.The models are for discrete and integrated circuit power semiconductor devices and related models. All of the models currently implemented in saber MAST HDL (Hardware Description Language) for use on the saber simulator available from Analogy; Inc. Compiled models are not available. The models can be translated into VHDL-AMS HDL, the new IEEE Standard Analog HDL or other HDLs for use on other simulators. Information on the possibilities for model support or translation into a standard HDL is

available. These models are available to the public without restrictions to promote their widespread use. Published model equations and source code is essential so models can easily be understood and installed on a variety of different simulators.

With source code available, users can also assist in identifying and fixing bugs in the models [6]. All these models are 1-D macromodels that depend on the one p-n junction diode as switching element. In addition, they fail to simulate the dynamic behavior at high frequency.

Due to their specific structures, the power devices need special models different from those developed for low power electronics. The development of such special models is far from being simple as distributed nature of phenomena often determinates the dynamic response of the device. The solution to this problem is the 2-D models.

The electronic circuit simulation with the application of 2-D models distributed physical models of power semiconductor devices is very time-consuming and requires very strong computation tools. The physical models of bipolar devices are very complex because of big structure dimensions and high non-linear doping profile. Moreover, it is important to simulate power semiconductor devices with a realistic external circuit.

The development of a software that would enable to develop 2-D device models and then to use them in circuit simulation was started by Napieralski and Turowski [7] and continued by Grecki and jablonski [8]. In the developed software, the computation process can be performed in parallel in order to reduce the computation time. The acceleration of computation in the case of circuits containing 2-D distributed physical