بسم الله الرحمن الرحيم

MONA MAGHRABY

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

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شبكة المعلومات الجامعية

التوثيق الإلكتروني والميكروفيلم

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

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MONA MAGHRABY

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Design Automation of All Digital Phase Locked Loop

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by
Abdelrahman Samy Mostafa Mohamed Rizk
Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2016

Supervised By
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Dr. Hesham Abdel Salam Ahmed Omran

Cairo
3 July 2021

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Date: 3 July 2021

Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

In the recent years, the system on a chip (SoC) design has seen many advances due to the new technology nodes and the increase of system complexity. All-digital phase locked loop (ADPLL) usage gained more consideration in the advanced nodes SoCs, the building blocks of the ADPLL are mostly digital blocks, which gives it upper hand over the analog phase locked loop due to the easiness of integration, scalability with the technology nodes, flexibility of design and operation of the digital blocks, and immunity to supply noise and variations.

This thesis presents a design and optimization tool for the ADPLL system and circuits. The tool is implemented using Matlab scripts that create optimized design netlists and runs circuit simulator to simulate these netlists and verify the system requirements.

The thesis is divided into six chapters as listed below:

Chapter 1 This chapter is the introduction of the thesis. It starts with an introduction to the PLLs and ADPLL. Then the contributions of this thesis. Finally presenting the thesis organization.

Chapter 2 This chapter starts with literature review of the ADPLL system models, then discusses the used model and the tool's flow and the contributions to this model to determine the system parameters.

Chapter 3 In this chapter, the DCO architectures are discussed, and the automated design flow using g_m/ID methodology is presented. also the design flow of the capacitor banks is presented.

Chapter 4 In this chapter, the automated digital design flow for the digital blocks is presented. Starting from the circuits specifications, till the automatic synthesis, placement and routing of the circuits' RTL

Chapter 5 In this chapter design examples are implemented using the design tool. The system simulations are presented and the results are discussed.

Chapter 6 The conclusion of the thesis is given in this chapter, in addition to suggestions for future work.

Key words: All digital phase locked-loop (ADPLL), design automation, evolutionary design optimization methods, digital loop filter (DLF), phase noise, g_m/ID methodology, digitally controlled oscillator, design optimization, automatic placement and routing

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