شبكة المعلومات الجامعية

التوثيق الإلكتروني والميكروفيلم

بسم الله الرحمن الرحيم

HANAA ALY

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جامعة عين شمس

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قسم

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HANAA ALY

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Reference Oscillators for RF-PLL Systems

A Thesis submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Mohamed Salah Mohamed Eleraky

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2016

Supervised By

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Dr. Mohamed Ahmed Mohamed El-Nozahi

Cairo - (2021)

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications

Thesis title: **Reference Oscillators for RF-PLL Systems**

Submitted by: **Mohamed Salah Mohamed Eleraky**

Degree: **Master of Science in Electrical Engineering**

Abstract

Recently, low-power circuit design gains a big momentum as it considered as a key enabler for different applications, especially Internet of Things (IoT) systems. Moreover, low-power circuit design allows reducing the battery size by reducing the needed power consumption, which accordingly reduces the area/cost of these systems and enhance the battery lifetime. Typically, the receiver (RX) and the Transmitter (TX) within the wireless communication systems consume a significant fraction of power from the whole power consumption. Phased Locked Loop (PLL), which is a basic building block in any wireless communication systems for a precise clock generation, dominates the power consumption of the RX/TX. Moreover, the frequency divider and the Voltage-Controlled Oscillator (VCO) within the PLL dominates the power consumption of the PLL.

Consequently, in this thesis, a low-power, low area Phased Locked Loop is presented using 130nm CMOS technology. The proposed frequency synthesizer exploits the charge steering concept within the VCO and the frequency divider to reduce the power consumption of the entire PLL. The proposed PLL system is suitable not only for low-power systems but also for low supply voltage applications.

Charge steering based circuits are then implemented and designed to get an out-put frequency of 2.4 GHz from a 100 MHz reference signal. Simulations show a total power consumption of only 0.13 mW from a 1-V supply in 130nm CMOS technology. The PLL achieves a phase noise of -110 dBc/Hz at 1-MHz offset from the carrier signal, 2.4-GHz. The total root-mean-square jitter, σrms, in a frequency range of (10KHz to 40MHz) is 1743 fs, which yields a figure of merit (FOM) of -244dB.

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Thesis Summary

This dissertation is divided mainly into two parts as follows: the first part contains the fundamentals of PLL, which are introduced in Chapters 1, 2 and 3. While the second part introduces the novel work in the thesis and is discussed in Chapter 4. The thesis is composed of five chapters including lists of contents, figures, and tables as well as a list of references.

Chapter 1:

In this chapter, an introduction that briefly discusses the wireless technologies for IoT applications, focusing on the importance of using low-power techniques in the IoT circuits. Then, it follows a discussion in the power distribution in the PLLs. Eventually, the thesis outlines are presented.

Chapter 2:

This chapter discusses a quick revision of the PLLs role in wireless systems. Then, a brief revision of the basic concepts of each building block of the PLL are discussed. The revision includes a literature survey on the state-of-the-art of each of these building blocks. The vital focus of these survey is to be applicable for low-power wireless transceivers to support the extensive scale of the Internet of Things applications.

Chapter 3:

The system level design of charge pump based PLL using quantitative analysis in MATLAB is presented in this chapter. The analysis includes the linear model of the PLL and calculates the noise transfer function for each block of the PLL. Then, the PLL specifications are presented, which includes the distribution of the power and noise on the building blocks of the PLL to match the requirements of the IoT short-range wireless communication technologies. Eventually, behavioral modeling for the PLL blocks is presented and the simulations results are discussed.

Chapter 4:

This chapter includes the circuit implementation, design, and simulation results of each building block of the PLL. Also, a detailed discussion of the proposed novel low-power wide locking range frequency divider based is introduced. Then, a low-power charge steering based ring oscillator is introduced. Eventually, the PLL system integration results are presented with comparing the performance of the proposed PLL with the state of art PLLs.