شبكة المعلومات الجامعية

التوثيق الإلكتروني والميكروفيلم

# بسم الله الرحمن الرحيم


HANAA ALY

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# جامعة عين شمس

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# قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

# يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار

HANAA ALY


**AIN SHAMS UNIVERSITY**
**FACULTY OF ENGINEERING**
**Electronics Engineering and Electrical Communications**

# Low Power Circuits for High Speed Serial Links Transceivers

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by

**Muhamed Fouad Abdelazeem Ibrahim Allam**

Bachelor of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)
Faculty of Engineering, Ain Shams University, 2017

Supervised By

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**Dr. Hesham Abdelsalam Omran**

Cairo, 2021


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**Examiners' Committee**

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| **Prof. Mohamed Amin Ibrahim Dessouky**<br>Electronics Engineering and Electrical Communications<br>Faculty of Engineering, Ain Shams University. | ..... |
| **Dr. Sameh Assem Ibrahim**<br>Electronics Engineering and Electrical Communications<br>Faculty of Engineering, Ain Shams University. | ..... |

Date:6 July 2021

# Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

**Muhamed Fouad Abdelazeem Ibrahim Allam**

Signature

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**Date:** 20 April 2021

# Researcher Data

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**Field of specialization:** Electronics Engineering
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**Date of issued degree :** July 2017
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# Thesis Summary

## Summary

The thesis is divided into five chapters as listed below:

Chapter 1

This chapter introduces the dissertation and discusses the motivation for this work, followed by the thesis outline.

Chapter 2

This chapter provides a background to the topic, illustrating the operation and composition of serial link transceivers. It also includes a literature survey on the various types of the clock and data recovery (CDR) systems. In addition, a classification of the CDR systems based on the literature survey is provided. The CDR systems are classified according to the existence of feedback, the type of phase detectors (PD), the existence of reference clock and the method of its implementation.

Chapter 3

This chapter illustrates the linear models for each block in second-order BBPD-CDR including a newly proposed model for the decimator block. It also describes the full linear model of CDR used to calculate the jitter-transfer ($JTRAN$) and jitter-generation ($JGEN$). In addition, a derivation of an equation for calculating the jitter tolerance of the $2^{nd}$ order digital BBPD based CDR and a description of the operation of conventional decimation topologies and their effect on CDR systems' performance are provided.

Chapter 4

This chapter compares the most commonly used decimation topologies in CDR systems. It also provides an intuitive explanation for their effect on CDR jitter performance. The chapter also introduces a novel decimation topology to enhance the jitter performance of the CDR. In addition, the chapter describes the operation of conventional PI and focuses on the drawback of trigonometric PI (TPI) as well as linear PI (LPI). It also proposes a novel PI to handle the major issues in common PI designs and enhance the PI phase update rate

Chapter 5

This chapter validates the linear model proposed and illustrates the enhancement done in CDR jitter performance through MATLAB/Simulink simulations by the proposed decimation topology. The chapter provides the spices simulation results that prove the advantage of the proposed PI novel design.

Chapter 6

Finally, this chapter includes conclusions and suggestions for future work

Key words:

Digital Clock and Data Recovery, decimator, majority voter, jitter transfer ($JTRAN$), jitter generation ($JGEN$), jitter tolerance ($JTOL$), phase-interpolators (PI), high-linearity.

# Abstract

**Faculty of Engineering – Ain Shams University**
**Electronics and Communication Engineering Department**

Thesis title: **"Low Power Circuits for High-Speed Serial Link"**
Submitted by: **Muhamed Fouad Allam**
Degree: **Masters of Science in Electrical Engineering**

**Abstract**

This thesis presents a fully linear model of phase-interpolator-based bang bang digital Clock and Data Recovery System (CDR), enabling accurate estimation of jitter tolerance (JTOL) and jitter-transfer (JTRAN). The model is based on linearizing the decimator block in a stochastic sense —independent of the CDR loop dynamics—and deriving JTOL behaviour for digital CDR separately. This thesis also compares most commonly used decimator topologies and their effect on the CDR noise performance. Consequently, it proposes a new decimator topology to decouple the CDR JTOL from JTRAN, enhancing the CDR jitter peformance. The proposed model and the new decimator topology are both verified through MATLAB/Simulink simulation of the CDR, measuring the JTRAN and JTOL of the nonlinear model and comparing it to that of the proposed linear model. The objective of the thesis is driven by the need of accurately modeling the CDR and providing a simple an intuitive explanation for the nonlinear CDR blocks behavior and effect on the jitter performance of the CDR. The thesis also presents a fast-switching phase-interpolator (PI) operating at 5-GHz with superior linearity. The PI is designed for high bandwidth clock and data recovery (CDR) to enable high jitter-tolerance (JTOL) in serial-link applications. It is based on a current-switching topology to enable a high phase-update rate. It also employs an adaptive regenerative amplifier (ARA) to prevent amplitude-dependent delays. This PI consists of cascaded trigonometric phase-interpolator (TPI) and linear phase-interpolator (LPI) stages together with cross-coupled devices load to immensely enhance its linearity, enabling an 8-bit resolution with an integral nonlinearity (INL) of 0.5 LSB and differential nonlinearity (DNL)