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قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
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Memory/Bus Arbitration in Multiple-Bus Multiprocessor Systems

Thesis submitted in accordance with the requirements of the Department of Mathematics Faculty of Science, Minufiya University

for
M. Sc. degree in
Computer Science

BY
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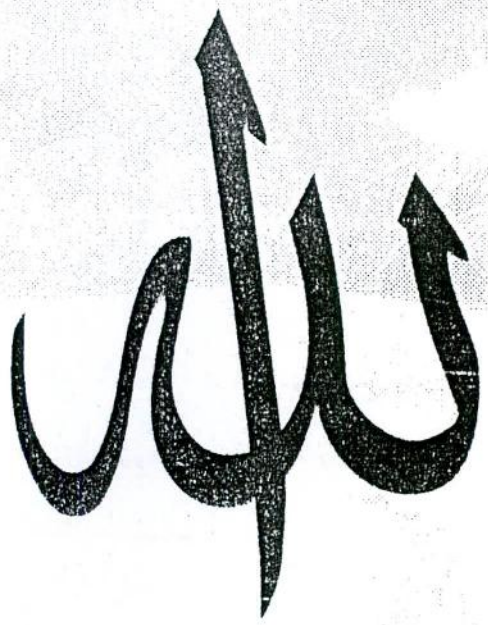

﴿وقل رب زدني علما﴾

﴿وما أوتيتم من العلم إلا قليلاً﴾

صدق الله العظيم

DEDICATION

To my lovely
My lifelong
My father, my mother
My brothers, my sisters

AND TO
MY WIFE

Who has spent two years from
her life to stand beside me,

SHERIF

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M.Sc. Thesis by

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ABSTRACT

The performance and behavior of tightly-coupled multiple-bus multiprocessor systems are modeled, developed and studied in this thesis. These systems consist of P processors and M memory modules. Each processor may have its own private cache and local I/O. Processors and memory modules are interconnected via B global buses, where each bus is connected to all processors and to all memory modules. Processors communicate through the shared memory modules. Such flexibility to access shared memory causing memory access conflicts that tend to degrade system performance. In these systems, processors may also contend for the path to the memory module. A theoretical stochastic model is developed for predicting the system performance in the presence of such memory/bus conflicts. Hardware arbiters are employed to resolve memory access conflicts and to allocate the available buses. The blocked requests due to memory/bus arbitration are not ignored but resubmitted during the next memory cycle. The performance of the modeled system is, generally, measured in terms of some popular criteria, such as *effective memory bandwidth* and *acceptance probability*. Many interconnection networks have been proposed for interconnecting processors and memory modules. These range from a single-bus to a fully connected crossbar. The simplest multiprocessor system and easiest to modify is one in which all processors are connected in parallel to *a single-bus* and all share this communication path to the memory modules. In this type of communication, arbitration hardware must be provided to

synchronize access to these memory modules by the different processors. Finally, simultaneous requests for the bus must be executed sequentially. The thesis considers this type of communication in the beginning. The performance is evaluated in terms of the effective memory bandwidth and the acceptance probability. Simulation studies are developed especially when the amount of processor-memory traffic is large. The case studies have shown that the bus is actually the performance-limiting factor in single-bus architectures for parallel processing. When the number of buses increased to approach the value B=min(P,M), the resulting special case is the crossbar network which is suffering only from memory conflicts. Simulation studies are presented in the thesis, and the results reveal that crossbars provide a maximum degree of performance. However, they scale up linearly in terms of performance, but at the expense of an O(P^2) complexity for a $P \times P$ crossbar. The general multiple-bus systems, when $B <$ min (P,M), are considered and their performance evaluated. Such general systems are suffering from both memory conflicts and bus arbitration. They strike a compromise between the price/performance alternatives offered by crossbars. Two models are considered. They are the even priority model and the prioritized model. In the even priority model, all processors are assumed to have the same priority level and the memory requests from each processor are assumed to be random, independent and uniformaly distributed over all the memory modules.

Prioritized multiple-bus multiprocessor systems are finally considered, in which each processor is assigned a priority level. In such systems, each processor will have different acceptance probability depending on its priority. Thus, the performance of each processor can be individually evaluated. The number of global buses can always play an effective part on the system performance as indicated from the results.

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