شبكة المعلومات الجامعية

بسم الله الرحمن الرحيم

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

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AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Energy Optimization for a Modern Embedded Microprocessor

A Thesis submitted in partial fulfillment of the requirements of
Master of Science in Electrical Engineering
(Electronics Engineering and Electrical Communications)

by
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Bachelor of Science in Electrical Engineering
(Communication Systems Engineering)
Faculty of Engineering, Ain Shams, 2016

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Cairo, 2021

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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

The design power dissipation became a major concern for IC designers as the product success depends on the battery lifetime, cooling management and thermal limits. Therefore, IC designers started to see the impact of power on design speed, design complexity, design area and fabrication cost. CAD tools could support power analysis and power optimization by different methodologies during the automated ASIC design flow.

ASIC design flow consists of several steps to design, optimize and verify the IC and a toolset is used for each step. For that purpose some open source EDA tools are developed and used by the students and researchers to learn and fabricate their own Integrated Circuits. This indicates how the EDA tool improvement community is growing in progress and it becomes flexible to design a hardened macro or even system on chip (SOC) with incorporating of these tools.

This thesis presents the digital ASIC implementation of RISC-V "DwarfRV32", which is an open source footprint for RV32I ISA using an open source PDK "sky130A". The design is implemented using two approaches, which are Openlane flow and Commercial tools. We then compare between the two flows on important parameters like power consumption and timing performance to get the most optimized design. Through all the design flow steps from RTL code to GDSII, each tool has its own methodologies and optimization techniques to get the most optimized design in power consumption, speed and area.

Summary

The development in the algorithms of electronic design automation (EDA) tools has made it appropriate to design application specific integrated circuit (ASIC) processors and carry out complete analysis of the corresponding parameters used for optimization. ASIC design flow could model the blocks as hardware accelerator that could be made part of a chip in a flexible way. Digital ASIC design flow is totally automated and at each step of this process, there is a need for a toolset. These steps are logic synthesis, physical implementation which includes floorplanning, placement, clock tree synthesis (CTS), routing and optimization, then static timing analysis (STA) and physical verification. STA is followed by power estimation techniques as power optimization became very important in modern nanometric technologies. Thus, each step in this flow is implemented such that the design critical parameters like timing, power and area could be optimized greatly with the aid of EDA tools.

Open source EDA is rapidly allowing new waves of innovation on many sides. For academic researchers, it speeds up the life cycle of scientific progress and makes research findings relevant to modern industry practices. For EDA professionals and the industrial ecosystem, open source EDA is a complement and enhancer to commercial EDA. For the IC design community, recent releases under permissive licenses make it possible to transfer ideas to a fabricated layout at no cost. In this thesis, we mainly concentrate on how the results of open source EDA tools, like OpenLane flow with its usage on digital ASIC design and optimization are reasonable and efficient, compared with the commercial flow.

This thesis presents the digital ASIC implementation of RISC-V "DwarfRV32". The design is implemented using two approaches, which are Openlane flow and Commercial tools. We then compare between the two flows on important parameters like timing performance and power consumption to get the most optimized design.

The thesis is divided into seven chapters as listed below:

Chapter 1: This chapter is the introduction of the thesis, it starts with an introduction to the microprocessor components, different ISA RISC and CISC classifications, RISC-V specifications, ASIC implementation advantage, then the thesis contributions, and the thesis organization.

Chapter 2: This chapter defines the design to be implemented dwarfRV32, its specifications and the PDK, Standard cell library to be used (SKYWATER SKY130A).

Chapter 3: This chapter defines the full ASIC implementation steps from RTL code to GDSII including synthesis, floorplan, powerplan, placement, clock tree synthesis and routing.

Chapter 4: In this chapter, the ASIC design implementation of RISC-V (dwarfRV32) using synopsys tools, optimizing and verifying the design on trade-off parameters power, area and timing.

Chapter 5: This chapter defines open source flow such as OpenLane to implement, optimize and verify our ASIC design implementation of RISC-V (dwarfRV32).

Chapter 6: In this chapter, a comparison is implemented between the OpenLane flow and Commercial flow in power consumption, timing and area with the same input setup.

Chapter 7: In this chapter, the conclusion of the thesis is given. Also suggestions for future work.

Keywords: ASIC, CAD, CTS, EDA, Floorplan, OpenLane, Optimization, Placement, Powerplan, RISC-V, Routing, STA, Synthesis.