شبكة المعلومات الجامعية

التوثيق الإلكتروني والميكروفيلم

بسم الله الرحمن الرحيم

HANAA ALY

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جامعة عين شمس

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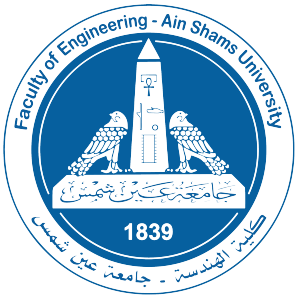
قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار

HANAA ALY



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Department of Electronics and Electrical Communication Engineering

Low Power Design for Dynamic Logic Circuits

A Thesis submitted in partial fulfillment of the requirements of
Doctor of Philosophy in Electrical Engineering
Department of Electronics and Electrical Communication Engineering

by
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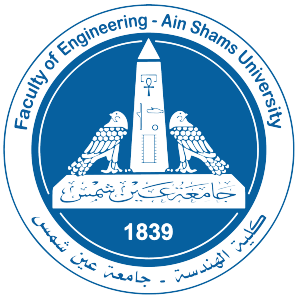
Cairo, 2021



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Statement

This thesis is submitted as a partial fulfillment of Doctor of Philosophy in Department of Electronics and Electrical Communication Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Designing low power circuits is a major target meanwhile. Governments and different initiatives encourage designing low power circuits to reduce power consumption worldwide. Customers are interested in low power designs due to different reasons as longer battery life. SoC can be implemented using dynamic and/or static CMOS logics. A dynamic CMOS logic uses two phases to evaluate a designed logic, which are: preparation phase and evaluation phases. The preparation phase is named pre-charge phase and pre-discharge phase for n-type and p-type dynamic logics, respectively. Dynamic power consumption of a dynamic logic increases when successive preparation and evaluation phases result in different voltage levels at its output node.

This research proposes new methods to reduce a circuit's power consumption by controlling the preparation and the evaluation phases of dynamic logics. New methods are proposed to design single stage and pipelined systems to produce circuits, which consume less power than circuits implemented using the traditional techniques. Different techniques are proposed to define which dynamic logics are recommended to be modified to reduce a circuit's power consumption. Modifying dynamic logics is also used to conditionally improving a circuit's speed. New methods, flip-flops, and latches are proposed to use new proposed preparation and evaluation controlled dynamic logics effectively by single and multi-stage systems. New approach and netlist diagram are proposed to highlight high power consumption parts of a design and illustrate it in a simple way to ease its analysis and improve its power consumption. Finally, a new flow is proposed to modify an implemented circuit to produce a better version, which consumes less power and operates at a higher speed.

Experimental results show the efficiency of the proposed techniques to reduce a circuit's power consumption and conditionally improving its speed. It also shows the ability of using the new techniques with currently used ones versus different and variant current and future operating conditions. The new proposed techniques are compared versus a new recently proposed power reduction technique. Comparison results using tiny, intermediate side, and large size designs show that the new proposed techniques give better results for power consumption, area, and speed aspects. The new proposed techniques show up to 59% power reduction compared to the traditional techniques with improving a circuit's performance by 3× of its original maximum operating frequency at the cost of an extra 12.3% increase in area.

Summary

A chip's power consumption and speed are critical aspects nowadays. Low power design is encouraged by many programs and initiatives to increase energy efficiency worldwide. CMOS technology is used nowadays to implement a high speed SoC. SoC can be designed using dynamic CMOS logics, or static CMOS logics, or combinations of both logics. Dynamic CMOS logics are usually used for custom design, but static CMOS ones are usually used by synthesis tools through standard cells.

Using dynamic logics usually results in extra power consumption compared to using static logics. Dynamic logics use two phases to evaluate a designed logic. The first phase can be named preparation phase as it prepares dynamic logics for the second phase. The preparation phase is named pre-charge phase and pre-discharge phase for n-type and p-type dynamic logics, respectively. Whereas, the second one is named evaluation phase as it is used to evaluate a designed logic. Using an uncontrolled dynamic logic usually leads to increasing power consumption if its inputs, at the currently executed evaluation phase, result in a different output voltage level compared to one defined at the preceding preparation phase. Accordingly, dynamic logics need a kind of control to avoid high power consumption.

This thesis proposes new flows, methodologies, and perspectives to reduce a design's power consumption and conditionally improving its speed. That is, it proposes new flows, which define dynamic logics that are recommended to be modified per a design and how to modify them to achieve the desired goals. It also presents two new methodologies to implement or/and modify a design for improving its specifications.

Two new modified dynamic logics are proposed to replace each Default Dynamic Logic (DDL), which are Evaluation phase Control Dynamic Logic (ECDL) and Preparation phase Control Dynamic Logic (PCDL). ECDL and PCDL reduce power consumption by controlling the evaluation phases and the preparation phases per a dynamic logic, respectively. New methods are proposed to define implementing each dynamic logic using ECDL, or PCDL, or DLL to improve its power consumption and speed. The new methods are based on probability, SystemVerilog CoverGroup (SVCG), and SystemVerilog Assertion (SVA). A new model has been proposed to convert SVCG to SVA to get use of SVA debugging methods to debug SVCG to help in defining dynamic logics that are recommended to be

modified to improve a circuit's specifications. A new netlist diagram generator and a new event type perspective have been proposed to easy analyzing a design, which results in extra power reduction.

Two new methodologies have been proposed to implement circuits using ECDL, or PCDL, or combinations of default and modified dynamic logics. The new methodologies are named Domain Isolation Methodology (DIM) and Pipe Domain Methodology (PDM). DIM is good for single stage systems and it is based on ECDL. Whereas, PDM is based on ECDL, PCDL, and DDL. Using DIM to implement pipelined systems results in extra power consumption and area compared to the default dynamic logic pipelined techniques. PDM addresses issues of DIM and it can implement single-stage and multi-stage systems efficiently. New enhanced latches and flip-flops are proposed by DIM to enable using ECDL by pipelined systems efficiently.

Experimental results show the effectiveness of the new proposed methodologies on improving circuits' power consumption and performance. They also show the ability of using the new techniques with the currently used ones versus current and future wide operating conditions. The thesis is divided into eight chapters as listed below:

Chapter 1 This chapter presents an overview of CMOS technology, motive for this research, and research contributions.

Chapter 2 This chapter shows currently used techniques to reduce power consumption of CMOS technology.

Chapter 3 This chapter presents technical background on SVCG, SVA, SV Specify Block (SVSB), and Clock Domain Crossing (CDC). These are used by our work to reduce circuits' power consumption and conditionally improving their speed.

Chapter 4 This chapter goes through our new digital implemental methodologies with showing the performance and the area analysis of our new power reduction techniques. That is, it surveys PCDL, ECDL, DIM, DIM issues, new enhanced C^2MOS latches and flip-flops, and PDM. In addition, it shows the performance and the area analysis of ECDL, PCDL, and new enhanced C^2MOS latches and flip-flops.

Chapter 5 It presents a new proposed event type perspective and a new netlist diagram generator that can be used to illustrate a design in a simple way with